1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

J110 MLB SCHEMATIC

09/25/14

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00384	1	SCHEM,MLB,J110	SCH	CRITICAL	
820-00164	1	PCBF,MLB,J110	PCB	CRITICAL	

DRAWING
TITLE MLB
ABBREV DRAWING
LAST MODIFIED<TS> Sep 25 14:26:29 2014

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

DRAWING TITLE: <PART_DESCRIPTION>

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 1 OF 120
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BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	ALTERNATE,COMMON,MLB_MISC,MLB_DEBUG:PVT,MLB_PROGPARTS
MLB_MISC	PP5V5 DCIN NO TBTHV P15V EDP CAM XTAL NO CAM WAKE NO APCLKRQ ISOL TPAD INTWAKE SHARED USB PWR S3 SD ON MLB VCORE FETS SSD LPSR S3
MLB_DEVEL:ENG	ALTERNATE,BKLT:ENG,XDP_CONN,DDRVREF_DAC,S0PGOOD_ISL,DBGLED,ISNS:ENG
MLB_DEVEL:PVT	XDP_CONN
MLB_DEBUG:ENG	XDP,SAMCONN
MLB_DEBUG:PVT	BKLT:PROD,XDP,SAMCONN,ISNS:ENG,DBGLED,XDP_CONN
MLB_DEBUG:PROD	BKLT:PROD,SAMCONN,XDP,ISNS:PROD

Current Sensor Configuration

BOM GROUP	BOM OPTIONS
ISNS:ENG	CPU H5 ISNS:YES CPUVR ISNS:YES DRAM ISNS:YES PSV6S ISNS:YES AIRPORT ISNS:YES SSD ISNS:YES LCDBKLT ISNS:YES PSV3S ISNS:YES 3V3S0 ISNS:YES OTHER H5 ISNS:YES CAM ISNS:YES CPUDDR ISNS:YES PANEL ISNS:YES
ISNS:PROD	CPU H5 ISNS:YES CPUVR ISNS:YES DRAM ISNS:YES PSV6S ISNS:NO AIRPORT ISNS:NO SSD ISNS:YES LCDBKLT ISNS:NO PSV3S ISNS:NO 3V3S0 ISNS:NO OTHER H5 ISNS:NO CAM ISNS:NO CPUDDR ISNS:NO PANEL ISNS:NO

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_4GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:ELPIDA_4GB
DDR3:ELPIDA_8GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:ELPIDA_8GB
DDR3:MICRON_4GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,DRAM_TYPE:MICRON_4GB
DDR3:MICRON_8GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,DRAM_TYPE:MICRON_8GB
DDR3:HYNIX_16GB	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:HYNIX_16GB
DDR3:SAMSUNG_16GB	RAMCFG0:L,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:SAMSUNG_16GB
DDR3:ELPIDA_16GB	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:ELPIDA_16GB
DDR3:MICRON_16GB	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:H,DRAM_TYPE:MICRON_16GB

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0915	1	EEPROM 4MBIT SPI 50MHZ 1 8V USON8	U2890	CRITICAL	TBTROM:BLANK
341S00159	1	T29 EEPROM FALCON RIDGE(V27 1) PROTO 0 J110/J113	U2890	CRITICAL	TBTROM:PROG
338S1214	1	IC SMC12 B1 40MHZ/50DMIPS MCU 157BGA	U5000	CRITICAL	SMC:BLANK
335S00006	1	IC SERIAL FLASH 64 MBIT 3V WSON QE 1	U6100	CRITICAL	BOOTROM MAC BLANK
335S00007	1	IC SERIAL FLASH 64 MBIT 3V WSON QE 1	U6100	CRITICAL	BOOTROM NUM BLANK
341S00153	1	IC EFI ROM(V8108) PROTO 0 J110/J113	U6100	CRITICAL	BOOTROM:PROG

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00029	1	BDW QGH9 D0 1 8 15W 2+2 0 7 4M B1168	U0500	CRITICAL	CPU:2.1GHZ
337S00073	1	BDW QGHB D0 1 6 15W 2+2 0 6 4M B1168	U0500	CRITICAL	CPU:1.6GHZ
338S00069	1	IC TBT FR 2C 28G 12X12 FC CSP TRAY	U2800	CRITICAL	
338S1264	1	IC BCM15700A2KFEB4G S2 CMRA 8X8 208FCBGA	U3900	CRITICAL	
607-6811	1	ASSEMBLY SUBASSY PCBA HALL EFFECT K99	J6955	CRITICAL	J110_MLB
946-5477	1	UV GLUE MLB J41 J43	GLUE	CRITICAL	
825-7670	1	LABEL,TEXT,MLB,K21/K78	LABEL		
376S00036	2	MOSFET N CH 25V 30A 9 6M 8P 3 3X3 3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:REN
376S00037	2	MOSFET N CH 25V 30A 6 1M 8P 3 3X3 3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:REN
376S1194	2	MOSFET N CH 30V 15 3A 12M 8P 3 3X3 3 DFN	Q7310,Q7320	CRITICAL	VCORE_FET:VSHY
376S1193	2	MOSFET N CH 30V 22A 6 0M 8P 3 3X3 3 DFN	Q7311,Q7321	CRITICAL	VCORE_FET:VSHY
900-0090	1		SOLDERPASTE	CRITICAL	
825-7987	1	LABEL,MLB,J41/J43	NEW_LABEL		

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0677	4	IC SDRAM 8Gb LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE HYNIX 4GB
333S0681	4	IC SDRAM 16Gb LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE HYNIX 8GB
333S00001	4	IC SDRAM 23NM 8GB LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE SAMSUNG 4GB
333S00003	4	IC SDRAM 23NM 16GB LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE SAMSUNG 8GB
333S0793	4	IC SDRAM 8Gb LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE ELPIDA 4GB
333S0791	4	IC SDRAM 16Gb LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE ELPIDA 8GB
333S0793	4	IC SDRAM 8Gb LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE MICRON 4GB
333S0791	4	IC SDRAM 16GB LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE MICRON 8GB
333S0789	4	IC SDRAM 25nm 32Gb LPDDR3 1600 178P FBGA	U2300 U2400 U2500 U2600	CRITICAL	DRAM TYPE ELPIDA 16GB

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

SIZE	CFG 3	CFG 2
4GB	0	0
8GB	0	1
16GB	1	0
RSVD	1	1

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1032	376S0855		ALL	Toshiba alt for Diodes dual
376S1129	376S0855		ALL	NXP alt for Diodes dual
376S1089	376S1128		ALL	NXP alt for Diodes single
138S0684	138S0660		ALL	Murata alt to Taiyo Yuden
138S0703	138S0648		ALL	Murata alt to Taiyo Yuden
152S0586	152S1301		ALL	Gale/Vishay alt to Cyntec
372S0186	372S0185		ALL	NXP alt to Diodes
197S0479	197S0478		ALL	20Mhz Epson alt to NDK
376S1053	376S0604		ALL	Diodes alt to Fairchild
371S0713	371S0558		ALL	Diodes alt to ST Micro
128S0371	128S0376		ALL	Kemet alt to Sanyo
152S1821	152S1757		ALL	Cyntec alt to NEC
197S0480	197S0343		ALL	NDK crystal alt to TXC
197S0481	197S0343		ALL	Epson crystal alt to TXC
107S0254	107S0241		ALL	Cyntec sense R alt to TFT
353S3452	353S1286		ALL	Maxim alt to Microchip
128S0386	128S0284		ALL	Kemet alt to Sanyo
128S0397	128S0325		ALL	Kemet alt to Sanyo
377S0155	377S0104		ALL	OnSemi alt to Infineon
128S0398	128S0220		ALL	Kemet alt to Sanyo
197S0542	197S0544		ALL	NDK alt to TXC
197S0545	197S0544		ALL	Epson alt to TXC
138S0681	138S0638		ALL	Taiyo alt to Samsung
138S0841	138S0638		ALL	Murata alt to Samsung
376S00014	376S0761		ALL	Renesas alt to Vishay
152S1876	152S1804		ALL	TDK alt to Toko
107S0255	107S0240		ALL	Cyntec alt to TFT
107S0250	107S0248		ALL	Cyntec alt to TFT
870-5074	870-1938		ALL	ALT POGO PIN W 0 CAP
870-5071	870-1940		ALL	ALT POGO PIN W 0 CAP
860-3428	860-1327		ALL	ALT STANDOFF W 0 MYLAR
860-3690	860-1328		ALL	ALT STANDOFF W 0 MYLAR
333S0787	333S0677	DRAM TYPE HYNIX 4GB	ALL	ALT STANDOFF W 0 MYLAR
333S0785	333S0681	DRAM TYPE HYNIX 8GB	ALL	ALT STANDOFF W 0 MYLAR

SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013

PAGE TITLE: BOM Configuration

Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-00613	PCBA,MLB,BETTER,HY-4GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_4GB,ALTERNATE
639-00614	PCBA,MLB,BETTER,HY-8GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:HYNIX_8GB,ALTERNATE
639-00616	PCBA,MLB,BETTER,SM-4GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:SAMSUNG_4GB,ALTERNATE
639-00617	PCBA,MLB,BETTER,SM-8GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:SAMSUNG_8GB,ALTERNATE
639-00621	PCBA,MLB,BETTER,EL-4GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_4GB
639-00622	PCBA,MLB,BETTER,EL-8GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_8GB
639-00695	PCBA,MLB,BETTER,EL-16GB,X430	MLB_CMNPTS,CPU:1.6GHZ,DDR3:ELPIDA_16GB
685-00043	CMN PTS,PCBA,MLB,X430	MLB_COMMON,J110_MLB
685-00044	VCORE FET,REN,X430	VCORE_FET:REN
685-00045	VCORE FET,VSHY,X430	VCORE_FET:VSHY

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-00044	685-00045		ALL	Renesas alt to Vishay
333S0704	333S0700		ALL	Elpida CAM DRAM alt to Hynix

BOM Groups

BOM GROUP	BOM OPTIONS
MLB_PROGPARTS	BOOTROM:PROG,SMC:PROG,TBTROM:PROG

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00147	1	IC SMC A3 EXT Vxxxx PROTO 0 J110	U5000	CRITICAL	SMC:PROG

Sub-BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00043	1	CMN PTS,PCBA,MLB,J110	CMNPTS	CRITICAL	MLB_CMNPTS
685-00045	1	VCORE FET,VSHY,J110	VCOREFETS	CRITICAL	VCORE_FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: BOM Variants

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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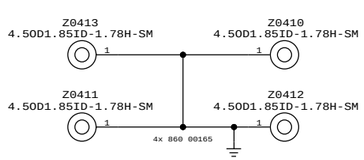
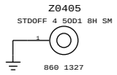
PD Module Parts

806-5107	1	CAN,TOPSIDE,ALT,J41/J43	TBTTOPSIDE 2P FENCE	CRITICAL	
806-5108	1	CAN TOPSIDE COVER ALT J41/J43	TBTTOPSIDE 2P COVER	CRITICAL	
806-3142	1	CAN,TBT,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN,COVER,TBT,J11/J13	TBTCOVER	CRITICAL	
806-3216	1	CAN,MDP,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB,MLB,J11/J13	USBCAN	CRITICAL	
725-1792	1	INSULATOR,CPU,J41/J43	CPU_INSULATOR	CRITICAL	

CPU Heat Sink Mounting Bosses

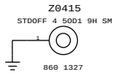


Fan Boss



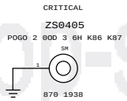
X21 Boss

SSD Boss

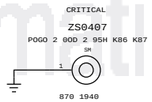


EMI I/O Pogo Pins

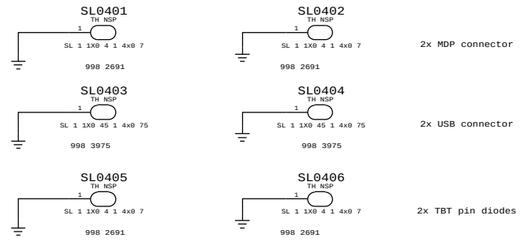
DisplayPort Pogo



USB/SD Card Pogo



Can Slots



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PAGE TITLE: PD Parts

Apple Inc.

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DDI Port Assignments:

TBT Sink 0

TBT Sink 1
(MUXed with HDMI
if necessary)

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 1 OF 19

DP_TBTSNK0_ML_C_N<0>	C54	DDI1_TXN0			
DP_TBTSNK0_ML_C_P<0>	C55	DDI1_TXP0			
DP_TBTSNK0_ML_C_N<1>	B58	DDI1_TXN1			
DP_TBTSNK0_ML_C_P<1>	C58	DDI1_TXP1			
DP_TBTSNK0_ML_C_N<2>	B55	DDI1_TXN2			
DP_TBTSNK0_ML_C_P<2>	A55	DDI1_TXP2			
DP_TBTSNK0_ML_C_N<3>	A57	DDI1_TXN3			
DP_TBTSNK0_ML_C_P<3>	B57	DDI1_TXP3			
DP_TBTSNK1_ML_C_N<0>	C51	DDI2_TXN0			
DP_TBTSNK1_ML_C_P<0>	C50	DDI2_TXP0			
DP_TBTSNK1_ML_C_N<1>	C53	DDI2_TXN1			
DP_TBTSNK1_ML_C_P<1>	B54	DDI2_TXP1			
DP_TBTSNK1_ML_C_N<2>	C49	DDI2_TXN2			
DP_TBTSNK1_ML_C_P<2>	B50	DDI2_TXP2			
DP_TBTSNK1_ML_C_N<3>	A53	DDI2_TXN3			
DP_TBTSNK1_ML_C_P<3>	B53	DDI2_TXP3			
		EDP_RCOMP	D20	MCP_EDP_RCOMP	
		EDP_DISP_UTIL	A43	TP_EDP_DISP_UTIL	

	EDP_TXN0	C45	DP_INT_ML_C_N<0>	58 65
	EDP_TXP0	B46	DP_INT_ML_C_P<0>	58 65
	EDP_TXN1	A47	NC_INT_ML_CN<1>	62
	EDP_TXP1	B47	NC_INT_ML_CP<1>	62
	EDP_TXN2	C47	NC_INT_ML_CN<2>	62
	EDP_TXP2	C46	NC_INT_ML_CP<2>	62
	EDP_TXN3	A49	NC_INT_ML_CN<3>	62
	EDP_TXP3	B49	NC_INT_ML_CP<3>	62
	EDP_AUXN	A45	DP_INT_AUXCH_C_N	58 65
	EDP_AUXP	B45	DP_INT_AUXCH_C_P	58 65

eDP Port Assignment:

Internal panel

PPVCOMP_S0_CPU 8

R0530
24.9
1%
1/20W
MF
201

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 17 OF 19

MCP_DC_AW2_AY2	TRUE	AY2	DAISY_CHAIN_NCTF			
MCP_DC_AW3_AY3	TRUE	AY3	DAISY_CHAIN_NCTF			
MCP_DC_AY60		AY60	DAISY_CHAIN_NCTF			
MCP_DC_AW61_AY61	TRUE	AY61	DAISY_CHAIN_NCTF			
MCP_DC_AW62_AY62	TRUE	AY62	DAISY_CHAIN_NCTF			
MCP_DC_B2		B2	DAISY_CHAIN_NCTF			
MCP_DC_A3_B3	TRUE	B3	DAISY_CHAIN_NCTF			
MCP_DC_A61_B61	TRUE	B61	DAISY_CHAIN_NCTF			
MCP_DC_B62_B63	TRUE	B62	DAISY_CHAIN_NCTF			
		B63	DAISY_CHAIN_NCTF			
MCP_DC_C1_C2	TRUE	C1	DAISY_CHAIN_NCTF			
		C2	DAISY_CHAIN_NCTF			

		DAISY_CHAIN_NCTF	A3	TRUE	MCP_DC_A3_B3
		DAISY_CHAIN_NCTF	A4		MCP_DC_A4
		DAISY_CHAIN_NCTF	A60		MCP_DC_A60
		DAISY_CHAIN_NCTF	A61	TRUE	MCP_DC_A61_B61
		DAISY_CHAIN_NCTF	A62		MCP_DC_A62
		DAISY_CHAIN_NCTF	AV1		MCP_DC_AV1
		DAISY_CHAIN_NCTF	AW1		MCP_DC_AW1
		DAISY_CHAIN_NCTF	AW2	TRUE	MCP_DC_AW2_AY2
		DAISY_CHAIN_NCTF	AW3	TRUE	MCP_DC_AW3_AY3
		DAISY_CHAIN_NCTF	AW61	TRUE	MCP_DC_AW61_AY61
		DAISY_CHAIN_NCTF	AW62	TRUE	MCP_DC_AW62_AY62
		DAISY_CHAIN_NCTF	AW63		MCP_DC_AW63

TP0531 (TP P6)
TP0501 (TP P6)

TP0500 (TP P6)
TP0510 (TP P6)
TP0511 (TP P6)
TP0520 (TP P6)
TP0521 (TP P6)
TP0530 (TP P6)

MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
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SPARE

NC	AT2	RSVD	RSVD	N23 NC
NC	AU44	RSVD	RSVD	R23 NC
NC	AV44	RSVD	RSVD	T23 NC
NC	D15	RSVD	RSVD	U10 NC
NC	F22	RSVD	RSVD	AL1 NC
NC	H22	RSVD	RSVD	AM11 NC
NC	J21	RSVD	RSVD	AP7 NC
			RSVD	AU10 NC
			RSVD	AU15 NC
			RSVD	AW14 NC
			RSVD	AY14 NC

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE
CPU GFX/NCTF/RSVD

Apple Inc.

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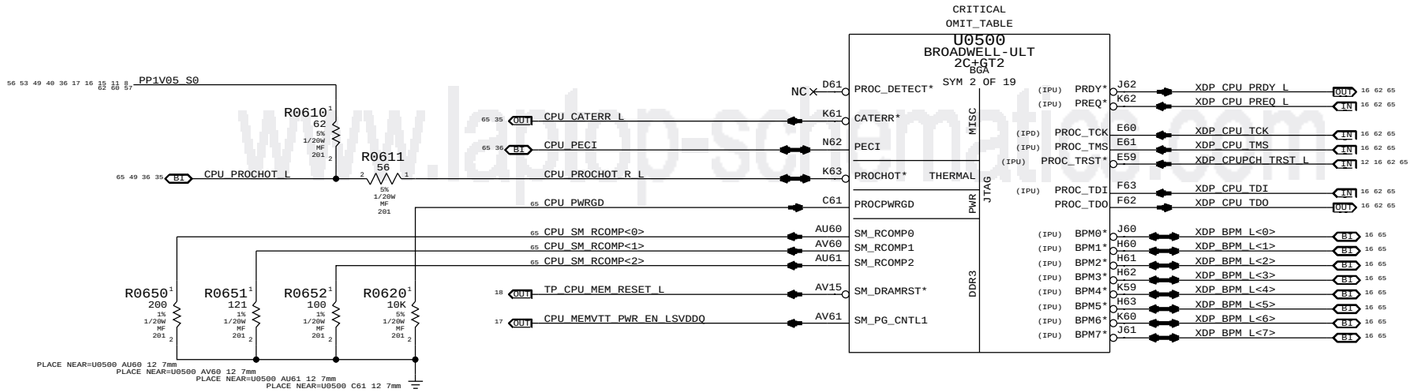
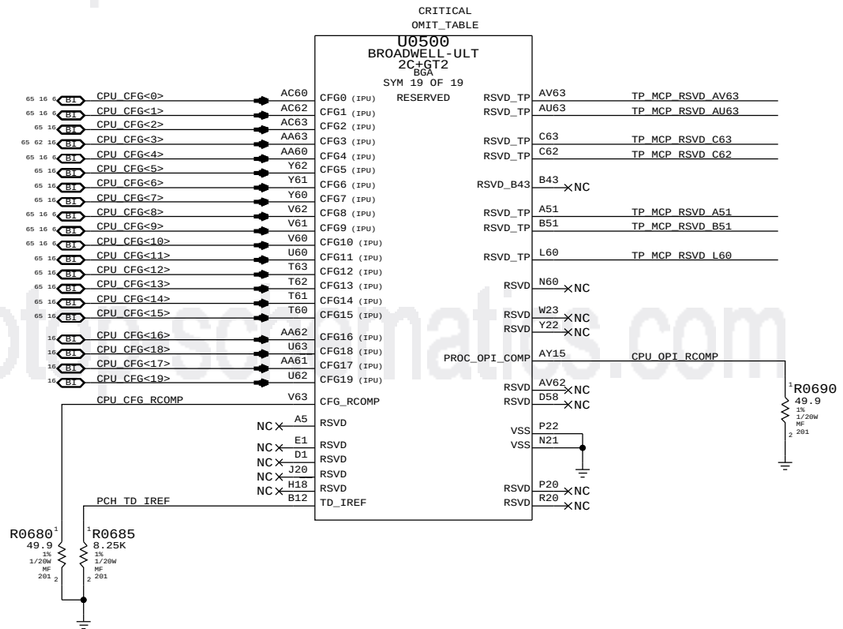
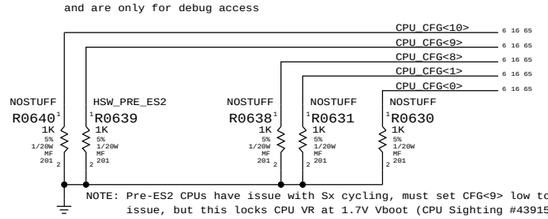


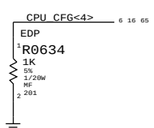


CFG<10>:SAFE MODE BOOT — 1 = NORMAL OPERATION — 0 = POWER FEATURES NOT ACTIVE
CFG<9> :NO SVID-CAPABLE VR — 1 = VR SUPPORTS SVID — 0 = VR DOES NOT SUPPORT SVID
CFG<8> :ALLOW NOA ON LOCKED UNITS — 1 = NORMAL OPERATION — 0 = NOA ALWAYS UNLOCKED
CFG<4> :eDP ENABLE/DISABLE — 1 = DISABLED — 0 = ENABLED
CFG<1> :PCH-LESS MODE — 1 = NORMAL OPERATION — 0 = PCH-LESS MODE
CFG<0> :RESET SEQUENCE STALL — 1 = NORMAL OPERATION — 0 = STALL AFTER PCU PLL LOCK

These can be placed close to J1800
and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE
CPU Misc/JTAG/CFG/RSVD

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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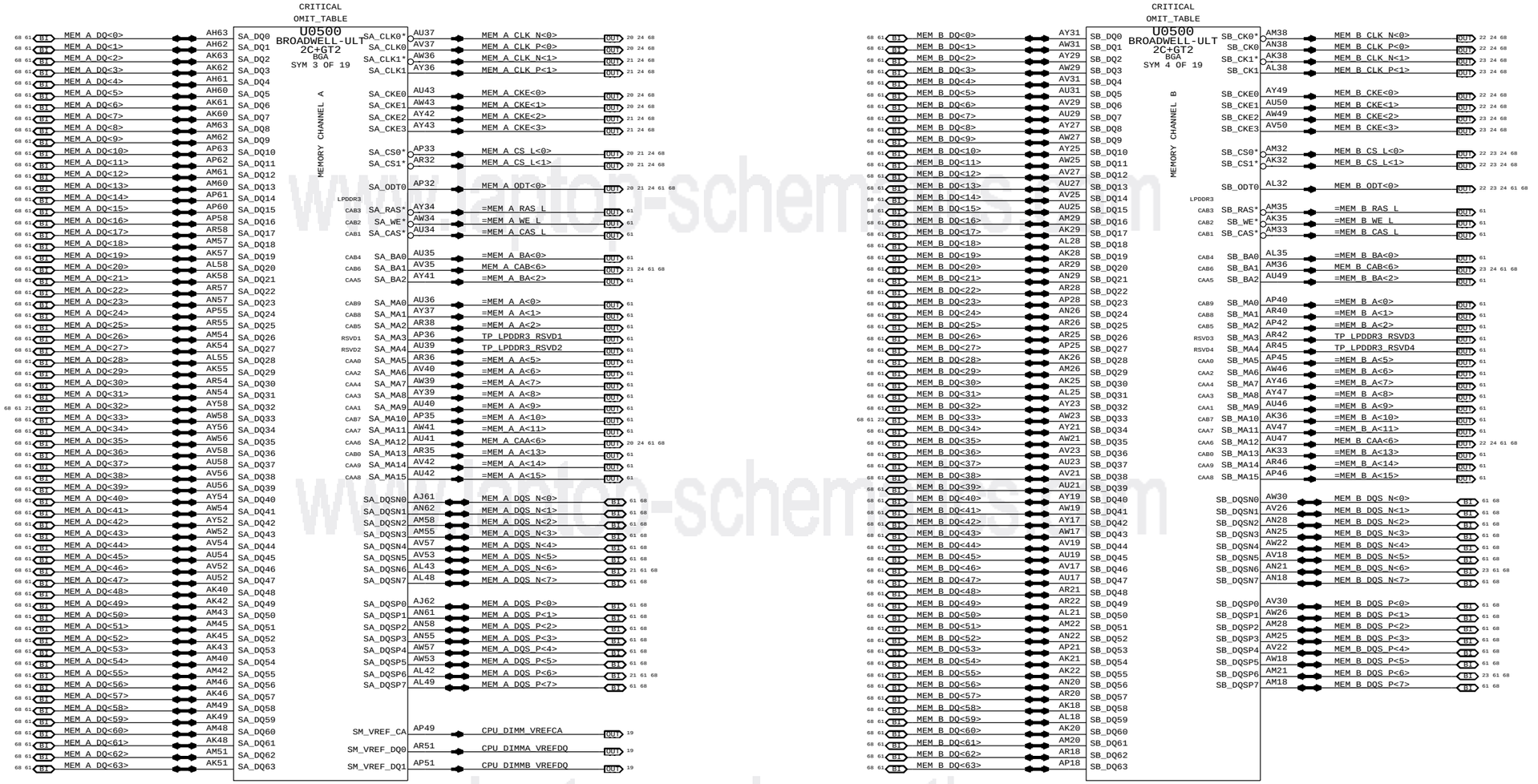

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE

CPU DDR3/LPDDR3 Interfaces

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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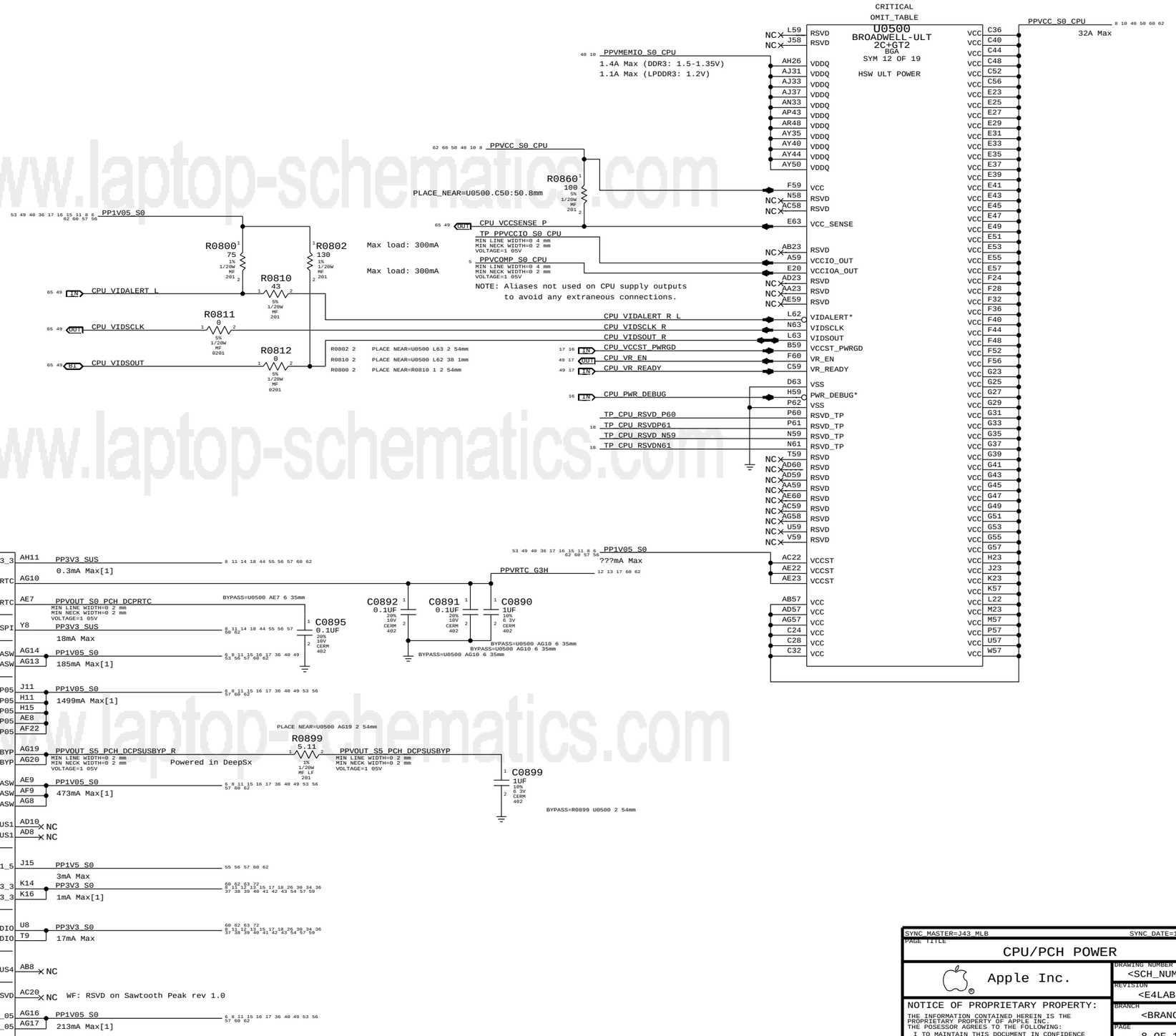
HSW-ULT current estimates from Haswell Mobile ULT Processor EDS vol 1, doc #502406, v0.9.
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0.
Note [1] current numbers from clarification email, from Srini, dated 9/10/2012 2:11pm.



SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012

PAGE TITLE: CPU/PCH POWER

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 8 OF 120
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CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 14 OF 19

A11	VSS	VSS	AJ35
A14	VSS	VSS	AJ39
A18	VSS	VSS	AJ41
A24	VSS	VSS	AJ43
A28	VSS	VSS	AJ45
A32	VSS	VSS	AJ47
A36	VSS	VSS	AJ50
A40	VSS	VSS	AJ52
A44	VSS	VSS	AJ54
A48	VSS	VSS	AJ56
A52	VSS	VSS	AJ58
A56	VSS	VSS	AJ60
AA1	VSS	VSS	AJ63
AA58	VSS	VSS	AK23
AB10	VSS	VSS	AK3
AB20	VSS	VSS	AK52
AB22	VSS	VSS	AL10
AB7	VSS	VSS	AL13
AC61	VSS	VSS	AL17
AD21	VSS	VSS	AL20
AD3	VSS	VSS	AL22
AD63	VSS	VSS	AL23
AE10	VSS	VSS	AL26
AE5	VSS	VSS	AL29
AE58	VSS	VSS	AL31
AF11	VSS	VSS	AL33
AF12	VSS	VSS	AL36
AF14	VSS	VSS	AL39
AF15	VSS	VSS	AL40
AF17	VSS	VSS	AL45
AF18	VSS	VSS	AL46
AG1	VSS	VSS	AL51
AG11	VSS	VSS	AL52
AG21	VSS	VSS	AL54
AG23	VSS	VSS	AL57
AG60	VSS	VSS	AL60
AG61	VSS	VSS	AL61
AG62	VSS	VSS	AM1
AG63	VSS	VSS	AM17
AH17	VSS	VSS	AM23
AH19	VSS	VSS	AM31
AH20	VSS	VSS	AM52
AH22	VSS	VSS	AN17
AH24	VSS	VSS	AN23
AH28	VSS	VSS	AN31
AH30	VSS	VSS	AN32
AH32	VSS	VSS	AN35
AH34	VSS	VSS	AN36
AH36	VSS	VSS	AN39
AH38	VSS	VSS	AN40
AH40	VSS	VSS	AN42
AH42	VSS	VSS	AN43
AH44	VSS	VSS	AN45
AH49	VSS	VSS	AN46
AH51	VSS	VSS	AN48
AH53	VSS	VSS	AN49
AH55	VSS	VSS	AN51
AH57	VSS	VSS	AN52
AJ13	VSS	VSS	AN60
AJ14	VSS	VSS	AN63
AJ23	VSS	VSS	AN7
AJ25	VSS	VSS	AP10
AJ27	VSS	VSS	AP17
AJ29	VSS	VSS	AP20

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 15 OF 19

AP22	VSS	VSS	AV59
AP23	VSS	VSS	AV8
AP26	VSS	VSS	AW16
AP29	VSS	VSS	AW24
AP3	VSS	VSS	AW33
AP31	VSS	VSS	AW35
AP38	VSS	VSS	AW37
AP39	VSS	VSS	AW4
AP48	VSS	VSS	AW40
AP52	VSS	VSS	AW42
AP54	VSS	VSS	AW44
AP57	VSS	VSS	AW47
AR11	VSS	VSS	AW50
AR15	VSS	VSS	AW51
AR17	VSS	VSS	AW59
AR23	VSS	VSS	AW60
AR31	VSS	VSS	AY11
AR33	VSS	VSS	AY16
AR39	VSS	VSS	AY18
AR43	VSS	VSS	AY22
AR49	VSS	VSS	AY24
AR5	VSS	VSS	AY26
AR52	VSS	VSS	AY30
AT13	VSS	VSS	AY33
AT35	VSS	VSS	AY4
AT37	VSS	VSS	AY51
AT40	VSS	VSS	AY53
AT42	VSS	VSS	AY57
AT43	VSS	VSS	AY59
AT46	VSS	VSS	AY6
AT49	VSS	VSS	B20
AT61	VSS	VSS	B24
AT62	VSS	VSS	B26
AT63	VSS	VSS	B28
AU1	VSS	VSS	B32
AU16	VSS	VSS	B36
AU18	VSS	VSS	B4
AU20	VSS	VSS	B40
AU22	VSS	VSS	B44
AU24	VSS	VSS	B48
AU26	VSS	VSS	B52
AU28	VSS	VSS	B56
AU30	VSS	VSS	B60
AU33	VSS	VSS	C11
AU51	VSS	VSS	C14
AU53	VSS	VSS	C18
AU55	VSS	VSS	C20
AU57	VSS	VSS	C25
AU59	VSS	VSS	C27
AV14	VSS	VSS	C38
AV16	VSS	VSS	C39
AV20	VSS	VSS	C57
AV24	VSS	VSS	D12
AV28	VSS	VSS	D14
AV33	VSS	VSS	D18
AV34	VSS	VSS	D2
AV36	VSS	VSS	D21
AV39	VSS	VSS	D23
AV41	VSS	VSS	D25
AV43	VSS	VSS	D26
AV46	VSS	VSS	D27
AV49	VSS	VSS	D29
AV51	VSS	VSS	D30
AV55	VSS	VSS	D31

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 16 OF 19

D33	VSS	VSS	H17
D34	VSS	VSS	H57
D35	VSS	VSS	J10
D37	VSS	VSS	J22
D38	VSS	VSS	J59
D39	VSS	VSS	J63
D41	VSS	VSS	K1
D42	VSS	VSS	K12
D43	VSS	VSS	L13
D45	VSS	VSS	L15
D46	VSS	VSS	L17
D47	VSS	VSS	L18
D49	VSS	VSS	L20
D5	VSS	VSS	L58
D50	VSS	VSS	L61
D51	VSS	VSS	L7
D53	VSS	VSS	M22
D54	VSS	VSS	N10
D55	VSS	VSS	N3
D57	VSS	VSS	P59
D59	VSS	VSS	P63
D62	VSS	VSS	R10
D8	VSS	VSS	R22
E11	VSS	VSS	R8
E17	VSS	VSS	T1
F20	VSS	VSS	T58
F26	VSS	VSS	U20
F30	VSS	VSS	U22
F34	VSS	VSS	U61
F38	VSS	VSS	U9
F42	VSS	VSS	V10
F46	VSS	VSS	V3
F50	VSS	VSS	V7
F54	VSS	VSS	W20
F58	VSS	VSS	W22
F61	VSS	VSS	Y10
G18	VSS	VSS	Y59
G22	VSS	VSS	Y63
G3	VSS		
G5	VSS	VSS	V58
G6	VSS	VSS	AH46
G8	VSS	VSS	V23
H13	VSS	VSS_SENSE	E62
		VSS	AH16

CPU_VCCSENSE_N — OUT — 49 65

R0960
100
5%
1/20W
MF
201
2

PLACE_NEAR=U0500.E62:50.8mm

SYNC_MASTER=J43_MLB SYNC_DATE=10/02/2012

PAGE TITLE
CPU/PCH GROUNDS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 1 0 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 10uF 0402 mirrored stuff, 1x 470uF stuff, 50x 10uF mirrored no stuff, 50x 10uF single sided no stuff

62 60 50 40 8 PPVCC_S0_CPU

NO STUFF C1000 10UF 20% 4V X6S 0402
NO STUFF C1001 10UF 20% 4V X6S 0402
NO STUFF C1002 10UF 20% 4V X6S 0402
NO STUFF C1003 10UF 20% 4V X6S 0402
NO STUFF C1004 10UF 20% 4V X6S 0402
NO STUFF C1005 10UF 20% 4V X6S 0402
NO STUFF C1006 10UF 20% 4V X6S 0402
NO STUFF C1007 10UF 20% 4V X6S 0402
NO STUFF C1008 10UF 20% 4V X6S 0402
NO STUFF C1009 10UF 20% 4V X6S 0402
NO STUFF C1010 10UF 20% 4V X6S 0402
NO STUFF C1011 10UF 20% 4V X6S 0402
NO STUFF C1012 10UF 20% 4V X6S 0402
NO STUFF C1013 10UF 20% 4V X6S 0402
NO STUFF C1014 10UF 20% 4V X6S 0402
NO STUFF C105A 10UF 20% 4V X6S 0402
CRITICAL C105B 10UF 20% 4V X6S 0402
CRITICAL C105C 10UF 20% 4V X6S 0402
NO STUFF C105D 10UF 20% 4V X6S 0402
NO STUFF C105E 10UF 20% 4V X6S 0402
CRITICAL C105F 10UF 20% 4V X6S 0402

NO STUFF C1015 10UF 20% 4V X6S 0402
NO STUFF C1016 10UF 20% 4V X6S 0402
NO STUFF C1017 10UF 20% 4V X6S 0402
NO STUFF C1018 10UF 20% 4V X6S 0402
NO STUFF C1019 10UF 20% 4V X6S 0402
NO STUFF C1020 10UF 20% 4V X6S 0402
NO STUFF C1021 10UF 20% 4V X6S 0402
NO STUFF C1030 10UF 20% 4V X6S 0402
NO STUFF C104A 10UF 20% 4V X6S 0402
NO STUFF C104B 10UF 20% 4V X6S 0402
NO STUFF C104C 10UF 20% 4V X6S 0402
CRITICAL C104D 10UF 20% 4V X6S 0402
NO STUFF C104E 10UF 20% 4V X6S 0402
CRITICAL C104F 10UF 20% 4V X6S 0402
CRITICAL C106A 10UF 20% 4V X6S 0402
NO STUFF C106B 10UF 20% 4V X6S 0402
NO STUFF C106C 10UF 20% 4V X6S 0402
NO STUFF C106D 10UF 20% 4V X6S 0402
NO STUFF C106E 10UF 20% 4V X6S 0402

CRITICAL C1070 10UF 20% 4V X6S 0402
CRITICAL C1071 10UF 20% 4V X6S 0402
NO STUFF C1072 10UF 20% 4V X6S 0402
NO STUFF C1073 10UF 20% 4V X6S 0402
NO STUFF C1074 10UF 20% 4V X6S 0402
NO STUFF C1075 10UF 20% 4V X6S 0402
CRITICAL C1076 10UF 20% 4V X6S 0402
CRITICAL C1077 10UF 20% 4V X6S 0402
NO STUFF C1078 10UF 20% 4V X6S 0402
NO STUFF C1079 10UF 20% 4V X6S 0402
NO STUFF C1080 10UF 20% 4V X6S 0402
NO STUFF C1081 10UF 20% 4V X6S 0402
NO STUFF C1082 10UF 20% 4V X6S 0402
CRITICAL C1083 10UF 20% 4V X6S 0402
CRITICAL C1084 10UF 20% 4V X6S 0402

CRITICAL C1085 10UF 20% 4V X6S 0402
CRITICAL C1086 10UF 20% 4V X6S 0402
CRITICAL C1087 10UF 20% 4V X6S 0402
NO STUFF C1088 10UF 20% 4V X6S 0402
NO STUFF C1089 10UF 20% 4V X6S 0402
NO STUFF C1090 10UF 20% 4V X6S 0402
CRITICAL C1091 10UF 20% 4V X6S 0402
CRITICAL C1092 10UF 20% 4V X6S 0402
NO STUFF C1093 10UF 20% 4V X6S 0402
NO STUFF C1094 10UF 20% 4V X6S 0402
NO STUFF C1095 10UF 20% 4V X6S 0402
NO STUFF C1096 10UF 20% 4V X6S 0402
CRITICAL C1097 10UF 20% 4V X6S 0402

NO STUFF C1022 10UF 20% 4V X6S 0402
NO STUFF C1023 10UF 20% 4V X6S 0402
NO STUFF C1024 10UF 20% 4V X6S 0402
NO STUFF C1025 10UF 20% 4V X6S 0402
NO STUFF C1026 10UF 20% 4V X6S 0402
NO STUFF C1027 10UF 20% 4V X6S 0402
NO STUFF C1028 10UF 20% 4V X6S 0402
NO STUFF C1029 10UF 20% 4V X6S 0402
NO STUFF C1032 10UF 20% 4V X6S 0402
NO STUFF C1033 10UF 20% 4V X6S 0402
NO STUFF C1034 10UF 20% 4V X6S 0402
NO STUFF C1035 10UF 20% 4V X6S 0402
NO STUFF C1036 10UF 20% 4V X6S 0402
NO STUFF C1037 10UF 20% 4V X6S 0402
NO STUFF C1038 10UF 20% 4V X6S 0402

NO STUFF C1039 10UF 20% 4V X6S 0402
NO STUFF C1044 10UF 20% 4V X6S 0402
NO STUFF C1045 10UF 20% 4V X6S 0402
NO STUFF C1046 10UF 20% 4V X6S 0402
NO STUFF C1047 10UF 20% 4V X6S 0402
NO STUFF C1048 10UF 20% 4V X6S 0402
NO STUFF C1049 10UF 20% 4V X6S 0402

NO STUFF C1056 10UF 20% 4V X6S 0402
NO STUFF C1057 10UF 20% 4V X6S 0402
NO STUFF C1058 10UF 20% 4V X6S 0402
NO STUFF C1059 10UF 20% 4V X6S 0402
NO STUFF C1062 10UF 20% 4V X6S 0402
NO STUFF C1063 10UF 20% 4V X6S 0402
NO STUFF C1064 10UF 20% 4V X6S 0402
NO STUFF C1065 10UF 20% 4V X6S 0402
NO STUFF C1066 10UF 20% 4V X6S 0402
NO STUFF C1067 10UF 20% 4V X6S 0402
NO STUFF C1068 10UF 20% 4V X6S 0402
NO STUFF C1069 10UF 20% 4V X6S 0402
NO STUFF C1098 10UF 20% 4V X6S 0402
NO STUFF C1099 10UF 20% 4V X6S 0402
NO STUFF C109A 10UF 20% 4V X6S 0402

NO STUFF C109B 10UF 20% 4V X6S 0402
NO STUFF C109C 10UF 20% 4V X6S 0402
NO STUFF C109D 10UF 20% 4V X6S 0402
NO STUFF C109E 10UF 20% 4V X6S 0402
NO STUFF C109F 10UF 20% 4V X6S 0402
NO STUFF C108A 10UF 20% 4V X6S 0402
NO STUFF C108B 10UF 20% 4V X6S 0402
NO STUFF C108C 10UF 20% 4V X6S 0402
NO STUFF C108D 10UF 20% 4V X6S 0402
NO STUFF C108E 10UF 20% 4V X6S 0402
NO STUFF C108F 10UF 20% 4V X6S 0402
NO STUFF C107A 10UF 20% 4V X6S 0402
NO STUFF C107B 10UF 20% 4V X6S 0402

CRITICAL C1031 470UF-0.0045OHM 20% 2.5V POLY TANT SM

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 4x 2.2uF 0402, 6x 10uF 0402, 2x 270uF B2 no stuff

40 8 PPVMEMIO_S0_CPU

C1040 2.2UF 20% 6.3V CERM 402 LF
C1041 2.2UF 20% 6.3V CERM 402 LF
C1042 2.2UF 20% 6.3V CERM 402 LF
C1043 2.2UF 20% 6.3V CERM 402 LF

C1050 10UF 20% 6.3V CERM X5R 0402 1
C1051 10UF 20% 6.3V CERM X5R 0402 1
C1052 10UF 20% 6.3V CERM X5R 0402 1
C1053 10UF 20% 6.3V CERM X5R 0402 1
C1054 10UF 20% 6.3V CERM X5R 0402 1
C1055 10UF 20% 6.3V CERM X5R 0402 1

C1060 270UF 20% 2V TANT CASE B2 SM
NO STUFF C1061 270UF 20% 2V TANT CASE B2 SM

2x Bulk nostuff per Harris Beach v1.0 schematic

SYNC_MASTER=LABEL_J41 SYNC_DATE=01/11/2013
PAGE TITLE: CPU Decoupling
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 10 OF 120
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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5
NO STUFF
C1200 1UF 10% 6.3V CERM 402
BYPASS=U0500 AH10 6 35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS
NO STUFF
C1202 0.1UF 20% 10V CERM 402
BYPASS=U0500 Y8 6 35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS
C1204 22UF 20% 6.3V X5R CERM 1 603
BYPASS=U0500 AC9 12 7mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS
C1206 1UF 10% 6.3V CERM 402
BYPASS=U0500 AH11 6 35mm

PCH VCCSDIO BYPASS
(PCH 3.3V/1.8V SDIO PWR)
PP3V3_S0
C1208 1UF 10% 6.3V CERM 402
BYPASS=U0500 U8 6 35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0SW_AUDIO_HDA
C1210 1UF 10% 6.3V CERM 402
BYPASS=U0500 AH14 6 35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0
C1212 22UF 20% 6.3V X5R CERM 1 603
BYPASS=U0500 V8 12 7mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0
C1214 0.1UF 20% 10V CERM 402
BYPASS=U0500 K14 6 35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
NO STUFF
C1250 22UF 20% 6.3V X5R CERM 1 603
C1251 1UF 10% 6.3V CERM 402
BYPASS=U0500 AE9 12 7mm
BYPASS=U0500 AE9 6 35mm

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0
C1255 10UF 20% 6.3V X5R 603
C1256 1UF 10% 6.3V CERM 402
C1257 1UF 10% 6.3V CERM 402
BYPASS=U0500 J11 12 7mm
BYPASS=U0500 J11 6 35mm
BYPASS=U0500 AE8 6 35mm

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe/SATA/USB3 PWR)
PP1V05_S0SW_PCH_HSIO
C1260 1UF 10% 6.3V CERM 402
C1261 1UF 10% 6.3V CERM 402
C1262 10UF 20% 6.3V CERM X5R 0402 1
BYPASS=U0500 K9 6 35mm
BYPASS=U0500 L10 6 35mm
BYPASS=U0500 M9 6 35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0
C1264 1UF 10% 6.3V CERM 402
BYPASS=U0500 AG16 6 35mm

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
PP1V05_S0
C1266 1UF 10% 6.3V CERM 402
C1267 1UF 10% 6.3V CERM 402
BYPASS=U0500 J17 6 35mm
BYPASS=U0500 R21 6 35mm

PP1V05_S0
??mA Max
R1270 0 5% 1/10W MF LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1270 2.2UH-240MA-0.221OHM 0603
C1270 47UF 20% 4V CERM X5R 0805 1
C1271 47UF 20% 4V CERM X5R 0805 1
C1272 1UF 10% 10V X5R 402
BYPASS=U0500 A20 12 7mm
BYPASS=U0500 A20 12 7mm
BYPASS=U0500 A20 6 35mm
PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
31mA Max

R1275 0 5% 1/10W MF LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.2 MM
VOLTAGE=1.05V
CRITICAL
L1275 2.2UH-240MA-0.221OHM 0603
C1275 47UF 20% 4V CERM X5R 0805 1
C1276 47UF 20% 4V CERM X5R 0805 1
C1277 1UF 10% 10V X5R 402
BYPASS=U0500 J18 12 7mm
BYPASS=U0500 J18 12 7mm
BYPASS=U0500 J18 6 35mm
PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
??mA Max

R1280 0 5% 1/10W MF LF 402
CRITICAL
NO STUFF
L1280 2.2UH-240MA-0.221OHM 0603
C1280 47UF 20% 4V CERM X5R 0805 1
C1281 47UF 20% 4V CERM X5R 0805 1
C1282 1UF 10% 10V X5R 402
BYPASS=U0500 AA21 12 7mm
BYPASS=U0500 AA21 12 7mm
BYPASS=U0500 AA21 6 35mm
PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
57mA Max

PP1V05_S0SW_PCH_HSIO
83mA Max
CRITICAL
L1290 2.2UH-240MA-0.221OHM 0603
C1290 47UF 20% 4V CERM X5R 0805 1
C1291 47UF 20% 4V CERM X5R 0805 1
C1292 1UF 10% 10V X5R 402
BYPASS=U0500 B11 12 7mm
BYPASS=U0500 B11 12 7mm
BYPASS=U0500 B11 6 35mm
PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0SW_PCH_VCCSATA3PLL
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
42mA Max

CRITICAL
L1295 2.2UH-240MA-0.221OHM 0603
C1295 47UF 20% 4V CERM X5R 0805 1
C1296 47UF 20% 4V CERM X5R 0805 1
C1297 1UF 10% 10V X5R 402
BYPASS=U0500 B18 12 7mm
BYPASS=U0500 B18 12 7mm
BYPASS=U0500 B18 6 35mm
PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0SW_PCH_VCCUSB3PLL
MIN LINE WIDTH=0.2 MM
MIN NECK WIDTH=0.075 MM
VOLTAGE=1.05V
41mA Max

LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srini, dated 9/10/2012 2:11pm.

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012
PAGE TITLE: PCH Decoupling
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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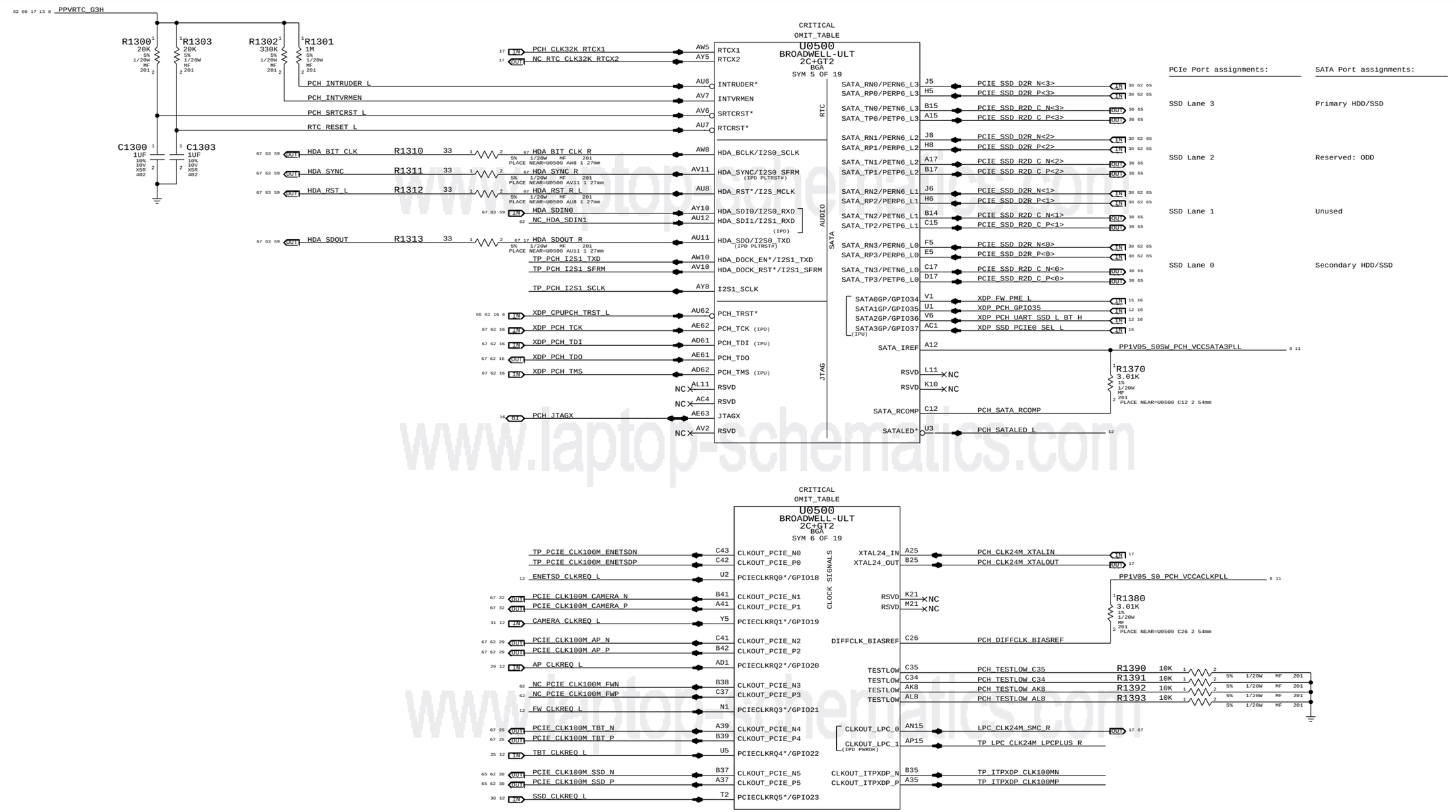
SHEET: 11 OF 73



SYNC MASTER=WILL_J43 SYNC DATE=12/17/2012

PAGE TITLE

PCH Audio/JTAG/SATA/CLK

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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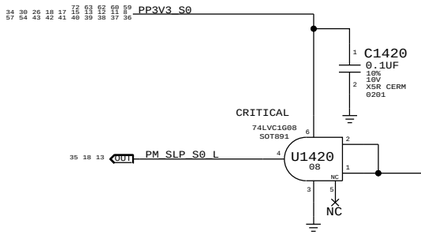
SLP_S0# Isolation



SLP_S0# can be driven high outside of S0
U1420 ensures signal will only be high in S0.

R1400 kept for debug purposes.

NO STUFF
R1400 0 5% 1/20W MF 0201

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 8 OF 19
SYSTEM POWER MANAGEMENT

37 IN	PCH_SUSACK_L	AK2	SUSACK* (IPU)	DSWVRMEN	AW7	PCH_DSWVRMEN
62 35 17 IN	PM_SYSRST_L	AC3	SYS_RESET*	DPWROK	AV5	PM_DSW_PWRGD
35 17 16 IN	PM_PCH_SYS_PWROK	AG2	SYS_PWROK	(IPD DeepSx) WAKE*	AJ5	PCIE_WAKE_L
17 13 IN	PM_PCH_PWROK	AY7	PCH_PWROK	CLKRUN*/GPIO32	V5	PM_CLKRUN_L
17 13 IN	PM_PCH_PWROK	AB5	APWROK	SUS_STAT*/GPIO61	AG4	LPC_PWRDWN_L
18 16 15 OUT	PLT_RESET_L	AG7	PLTRST*	SUSCLK/GPIO62	AE6	PM_CLK32K_SUSCLK_R
62 57 IN	PM_RSMRST_L	AW6	RSMRST*	SLP_S5*/GPIO63	AP5	PM_SLP_S5_L
37 OUT	PCH_SUSWARN_L	AV4	SUSWARN*/SUSPWRDNACK/GPIO30	SLP_S4*	AJ6	PM_SLP_S4_L
35 16 13 IN	PM_PWRBTN_L	AL7	PWRBTN* (IPU)	SLP_S3*	AT4	PM_SLP_S3_L
36 35 IN	SMC_ADAPTER_EN	AJ8	ACPRESENT/GPIO31 (IPD DeepSx)	SLP_A*	AL5	TP_PM_SLP_A_L
35 27 13 IN	PM_BATLOW_L	AN4	BATLOW*/GPIO72	SLP_SUS*	AP4	PM_SLP_SUS_L
PCH_PM_SLP_S0_L		AF3	SLP_S0*	SLP_LAN*	AJ7	TP_PCH_SLP_LAN_L
TP_PCH_SLP_WLAN_L		AM5	SLP_WLAN*/GPIO29			

PPVRTC_G3H
R1450 330K 5% 1/20W MF 201
R1451 100K 5% 1/20W MF 201

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 9 OF 19

54 OUT	EDP_BKLT_PWM	B8	EDP_BKLCTL	eDP SIDEBAND	DDPB_CTRLCLK	B9
54 13 OUT	EDP_BKLT_EN	A9	EDP_BKLEN		DDPB_CTRLDATA (IPD PLTRST#)	C9
58 13 OUT	EDP_PANEL_PWR	C6	EDP_VDDEN		DDPC_CTRLCLK	D9
					DDPC_CTRLDATA (IPD PLTRST#)	D11
26 13 IN	TBT_PWR_REQ_L	U6	PIRQA*/GPIO77	DISPLAY		
35 13 IN	SMC_RUNTIME_SCI_L	P4	PIRQB*/GPIO78			
62 13 IN	HDMITBTMUX_FLAG	N4	PIRQC*/GPIO79			
30 13 OUT	SSD_BOOT	N2	PIRQD*/GPIO80			
					DDPB_AUXN	C5
					DDPC_AUXN	B6
					DDPB_AUXP	B5
					DDPC_AUXP	A6
62 NC_PCI_PME_L		AD4	PME* (IPU)	PCI		
					DDPB_HPD	C8
					DDPC_HPD	A8
					EDP_HPD	D6
62 13 OUT	ODD_PWR_EN_L	U7	GPIO55			
62 13 OUT	HDMITBTMUX_LATCH	L1	GPIO52			
62 13 OUT	ENET_LOW_PWR	L3	GPIO54			
63 59 57 13 OUT	AUD_PWR_EN	R5	GPIO51			
62 13 OUT	AP_PCIE_DEV_WAKE	L4	GPIO53			

DP_TBTSNK0_DDC_CLK	OUT	18 28	
DP_TBTSNK0_DDC_DATA	BI	18 28	
DP_TBTSNK1_DDC_CLK	OUT	18	
DP_TBTSNK1_DDC_DATA	BI	18	
DP_TBTSNK0_AUXCH_C_N	BI	25 65	
DP_TBTSNK1_AUXCH_C_N	BI	18 25 65	
DP_TBTSNK0_AUXCH_C_P	BI	25 65	
DP_TBTSNK1_AUXCH_C_P	BI	18 25 65	
DP_TBTSNK0_HPD	IN	25	
DP_TBTSNK1_HPD	IN	18 25	
DP_INT_HPD	IN	58	

PP3V3_S5	8 11 15 16 17 18 28 29 40 52 55 56 57 58 60 62 72					
PP3V3_S0	8 11 12 13 15 17 18 26 30 34 36 37 38 39 40 41 42 43 54 57 59					
R1405	1K	5% 1/20W MF 201	PM_PWRBTN_L	13 16 35		
R1410	10K	5% 1/20W MF 201	PM_BATLOW_L	13 27 35		
R1452	10K	5% 1/20W MF 201	PCIE_WAKE_L	13 29 31 62		
R1455	10K	5% 1/20W MF 201	PM_CLKRUN_L	13 35 62		
R1460	100K	5% 1/20W MF 201	PM_SLP_S5_L	13 35 57		
R1461	100K	5% 1/20W MF 201	PM_SLP_S4_L	13 18 29 34 35 57		
R1462	100K	5% 1/20W MF 201	PM_SLP_S3_L	13 17 18 35 57		
R1463	100K	5% 1/20W MF 201	PM_SLP_S0_L	13 18 35		
R1464	100K	5% 1/20W MF 201	PM_SLP_SUS_L	13 40 57		
R1430	100K	5% 1/20W MF 201	EDP_BKLT_EN	13 54		
R1431	100K	5% 1/20W MF 201	EDP_PANEL_PWR	13 58		
R1440	100K	5% 1/20W MF 201	TBT_PWR_REQ_L	13 26		
R1441	100K	5% 1/20W MF 201	SMC_RUNTIME_SCI_L	13 35		
R1442	100K	5% 1/20W MF 201	HDMITBTMUX_FLAG	13 62		
R1443	100K	5% 1/20W MF 201	SSD_BOOT	13 30		
R1445	100K	5% 1/20W MF 201	ODD_PWR_EN_L	13 62		
R1446	100K	5% 1/20W MF 201	HDMITBTMUX_LATCH	13 62		
R1447	100K	5% 1/20W MF 201	ENET_LOW_PWR	13 62		
R1448	100K	5% 1/20W MF 201	AUD_PWR_EN	13 57 59 63		
R1449	100K	5% 1/20W MF 201	AP_PCIE_DEV_WAKE	13 62		

SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE
PCH PM/PCI/GFX

Apple Inc.

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PCIe Port Assignments:

Thunderbolt lane 0

Thunderbolt lane 1

Thunderbolt lane 2

Thunderbolt lane 3

AirPort

Reserved: FireWire

SD Card Reader
(& Ethernet if combo)

Camera

CRITICAL
OMIT_TABLE
U0500
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PCI-E
USB

67 25 IN	PCIE_TBT_D2R_N<0>	F10	PERN5_L0
67 25 IN	PCIE_TBT_D2R_P<0>	E10	PERP5_L0
67 25 OUT	PCIE_TBT_R2D_C_N<0>	C23	PETN5_L0
67 25 OUT	PCIE_TBT_R2D_C_P<0>	C22	PETP5_L0
67 25 IN	PCIE_TBT_D2R_N<1>	F8	PERN5_L1
67 25 IN	PCIE_TBT_D2R_P<1>	E8	PERP5_L1
67 25 OUT	PCIE_TBT_R2D_C_N<1>	B23	PETN5_L1
67 25 OUT	PCIE_TBT_R2D_C_P<1>	A23	PETP5_L1
67 25 IN	PCIE_TBT_D2R_N<2>	H10	PERN5_L2
67 25 IN	PCIE_TBT_D2R_P<2>	G10	PERP5_L2
67 25 OUT	PCIE_TBT_R2D_C_N<2>	B21	PETN5_L2
67 25 OUT	PCIE_TBT_R2D_C_P<2>	C21	PETP5_L2
67 25 IN	PCIE_TBT_D2R_N<3>	E6	PERN5_L3
67 25 IN	PCIE_TBT_D2R_P<3>	F6	PERP5_L3
67 25 OUT	PCIE_TBT_R2D_C_N<3>	B22	PETN5_L3
67 25 OUT	PCIE_TBT_R2D_C_P<3>	A21	PETP5_L3
67 62 29 IN	PCIE_AP_D2R_N	G11	PERN3
67 62 29 IN	PCIE_AP_D2R_P	F11	PERP3
67 29 OUT	PCIE_AP_R2D_C_N	C29	PETN3
67 29 OUT	PCIE_AP_R2D_C_P	B30	PETP3
62	NC_PCIE_FW_D2RN	F13	PERN4
62	NC_PCIE_FW_D2RP	G13	PERP4
62	NC_PCIE_FW_R2D_CN	B29	PETN4
62	NC_PCIE_FW_R2D_CP	A29	PETP4
66 63 IN	NC_USB3RPCIE_SD_D2RN	G17	PERN1/USB3RN3
66 63 IN	NC_USB3RPCIE_SD_D2RP	F17	PERP1/USB3RP3
66 63 OUT	NC_USB3RPCIE_SD_R2D_CN	C30	PETN1/USB3TN3
66 63 OUT	NC_USB3RPCIE_SD_R2D_CP	C31	PETP1/USB3TP3
67 32 IN	PCIE_CAMERA_D2R_N	F15	PERN2/USB3RN4
67 32 IN	PCIE_CAMERA_D2R_P	G15	PERP2/USB3RP4
67 32 OUT	PCIE_CAMERA_R2D_C_N	B31	PETN2/USB3TN4
67 32 OUT	PCIE_CAMERA_R2D_C_P	A31	PETP2/USB3TP4
NC		E15	RSVD
NC		E13	RSVD
	PCH_PCIE_RCOMP	A27	PCIE_RCOMP
		B27	PCIE_IREF

USB Port Assignments:

Ext A (LS/FS/HS)

Ext B (LS/FS/HS)

BT

IR

Trackpad

Unused

Reserved: Camera

Reserved: SD (HS)

USB2N0	AN8	USB_EXTA_N	33 66
USB2P0	AM8	USB_EXTA_P	33 66
USB2N1	AR7	USB_EXTB_N	59 63 66
USB2P1	AT7	USB_EXTB_P	59 63 66
USB2N2	AR8	USB_BT_N	29 66
USB2P2	AP8	USB_BT_P	29 66
USB2N3	AR10	NC_USB_IRN	62
USB2P3	AT10	NC_USB_IRP	62
USB2N4	AM15	USB_TPAD_N	34 62 66
USB2P4	AL15	USB_TPAD_P	34 62 66
USB2N5	AM13	TP_USB_5N	
USB2P5	AN13	TP_USB_5P	
USB2N6	AP11	NC_USB_CAMERAN	62
USB2P6	AN11	NC_USB_CAMERAP	62
USB2N7	AR13	NC_USB_SDN	62
USB2P7 (IPD)	AP13	NC_USB_SDP	62

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

USB3RN1	G20	USB3_EXTA_D2R_N	IN 33 66
USB3RP1	H20	USB3_EXTA_D2R_P	IN 33 66
USB3TN1	C33	USB3_EXTA_R2D_C_N	OUT 33 66
USB3TP1	B34	USB3_EXTA_R2D_C_P	OUT 33 66
USB3RN2	E18	USB3_EXTB_D2R_N	IN 59 63 66
USB3RP2	F18	USB3_EXTB_D2R_P	IN 59 63 66
USB3TN2	B33	USB3_EXTB_R2D_C_N	OUT 59 63 66
USB3TP2	A33	USB3_EXTB_R2D_C_P	OUT 59 63 66

USBRBIAS*	AJ10	66 PCH_USB_RBIAS	
USBRBIAS	AJ11		
RSVD	AN10	NC	
RSVD	AM10	NC	
OC0*/GPIO40	AL3	XDP_USB_EXTA_OC_L	IN 14 16 33
OC1*/GPIO41	AT1	XDP_USB_EXTB_OC_L	IN 14 16 59 63
OC2*/GPIO42	AH2	XDP_USB_EXTC_OC_L	IN 14 16
OC3*/GPIO43	AV3	XDP_USB_EXTD_OC_L	IN 14 16

PLACE NEAR=U0500.AJ10 2 54mm
R1570 22.6 1% 1/20W MF 201

11 8 PP1V05_S0SW_PCH_VCCUSB3PLL

R1500 3.01K 1% 1/20W MF 201
PLACE NEAR=U0500.A27 2 54mm

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
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LPC
SMBUS
SPI
C-LINK

67 62 35 BI	LPC_AD<0>	AU14	(IPU) LAD0
67 62 35 BI	LPC_AD<1>	AW12	LAD1
67 62 35 BI	LPC_AD<2>	AY12	LAD2
67 62 35 BI	LPC_AD<3>	AW11	LAD3
67 62 35 OUT	LPC_FRAME_L	AV12	LFRAME*
67 44 OUT	SPI_CLK_R	AA3	SPI_CLK (IPU)
67 44 OUT	SPI_CS0_R_L	Y7	SPI_CS0* (IPU)
TP_SPI_CS1_L		Y4	SPI_CS1* (IPU)
TP_SPI_CS2_L		AC2	SPI_CS2* (IPU)
67 44 BI	SPI_MOSI_R	AA2	SPI_MOSI (IPU/IPD)
67 44 BI	SPI_MISO	AA4	SPI_MISO (IPU)
67 44 14 BI	SPI_IO<2>	Y6	SPI_IO2 (IPU)
67 44 14 BI	SPI_IO<3>	AF1	SPI_IO3 (IPU)

	SMBALERT*/GPIO11	AN2	PCH_SMBALERT_L 14
	SMBCLK	AP2	SMBUS_PCH_CLK OUT 16 19 38 54 67
	SMBDATA	AH1	SMBUS_PCH_DATA BI 16 19 38 54 67
	SML0ALERT*/GPIO60	AL2	WOL_EN OUT 14 62
	SML0CLK	AN1	SML_PCH_0_CLK OUT 38 67
	SML0DATA	AK1	SML_PCH_0_DATA BI 38 67
	SML1ALERT*/PCHHOT*/GPIO73	AU4	PCH_SML1ALERT_L OUT 18 37
	SML1CLK_GPIO75	AU3	SMBUS_SMC_1_S0_SCL OUT 32 35 38 41 42 62 67 71
	SML1DATA/GPIO74	AH3	SMBUS_SMC_1_S0_SDA BI 32 35 38 41 42 62 67 71
(IPU/IPD)	CL_CLK	AF2	NC_CLINK_CLK 62
(IPU/IPD)	CL_DATA	AD2	NC_CLINK_DATA 62
	CL_RST*	AF4	NC_CLINK_RESET_L 62

SML1ALERT# pull-up not provided on this page, may be wire-ORed into other signals. Otherwise, 100k pull-up to 3.3V SUS required.

R1540	33	LPC_AD<0>	LPC_AD_R<0>
R1541	33	LPC_AD<1>	LPC_AD_R<1>
R1542	33	LPC_AD<2>	LPC_AD_R<2>
R1543	33	LPC_AD<3>	LPC_AD_R<3>
R1544	33	LPC_FRAME_L	LPC_FRAME_R_L

5% 1/20W MF 201

PP3V3_SUS 8 11 14 18 44 55 56 57 60 62
PP3V3_SUS 8 11 14 18 44 55 56 57 60 62

R1580	100K	XDP_USB_EXTA_OC_L	14 16 33
R1581	100K	XDP_USB_EXTB_OC_L	14 16 59 63
R1582	100K	XDP_USB_EXTC_OC_L	14 16
R1583	100K	XDP_USB_EXTD_OC_L	14 16
R1548	1K	SPI_IO<2>	14 44 67
R1549	1K	SPI_IO<3>	14 44 67
R1590	100K	PCH_SMBALERT_L	14
R1591	100K	WOL_EN	14 62

5% 1/20W MF 201

SYNC_MASTER=WILL_J43 SYNC_DATE=09/13/2012

PAGE TITLE
PCH PCIe/USB/LPC/SPI/SMBus

Apple Inc.

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BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

PP3V3_S0

RAMCFG3:H R1631 100K 5% 1/20W MF 201

RAMCFG2:H R1636 100K 5% 1/20W MF 201

RAMCFG1:H R1635 100K 5% 1/20W MF 201

RAMCFG0:H R1611 100K 5% 1/20W MF 201

XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3

GPIO12:

CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC

PP3V3_S3

SSD_LPSR:S3 R1696 100K 5% 1/20W MF 201

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT 2C+GT2
BGA
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XDP_PCH_GPIO76	P1	BMBUSY*/GPIO76
XDP_MLB_RAMCFG0	AU2	GPIO8
HDMITBTMUX_SEL_TBT	AM7	LAN_PHY_PWR_CTRL/GPIO12
TP_MEM_VDD_SEL_1V5_L	AD6	GPIO15 (IPD RSMRST#)
XDP_LPCPLUS_GPIO	Y1	GPIO16
XDP_PCH_GPIO17	T3	GPIO17
SD_RESET_L	AD5	GPIO24
SMC_WAKE_SCI_L	AN5	GPIO27 (IPD DeepSx)
TPAD_SPI_INT_GPIO28_L	AD7	GPIO28
TPAD_USB_IF_EN	AN3	GPIO26
SSD_PWR_EN	AG6	GPIO56
PCH_TBT_PCIE_RESET_L	AP1	GPIO57
HDD_PWR_EN	AL4	GPIO58
XDP_SDCONN_STATE_CHANGE_L	AT5	GPIO59
SD_PWR_EN	AK4	GPIO44
TBT_PWR_EN	AB6	GPIO47
XDP_JTAG_ISP_TCK	U4	GPIO48
XDP_JTAG_ISP_TDI	Y3	GPIO49
JTAG_TBT_TMS_PCH	P3	GPIO50
PCH_HSIO_PWR_EN	Y2	HSIOPC/GPIO71
TPAD_SPI_IF_EN	AT3	GPIO13
XDP_MLB_RAMCFG3	AH4	GPIO14
SPIROM_USE_MLB	AM4	GPIO25
CAMERA_PWR_EN_PCH	AG5	GPIO45
TPAD_SPI_INT_GPIO46_L	AG3	GPIO46
XDP_MLB_RAMCFG1	AM3	GPIO9
XDP_MLB_RAMCFG2	AM2	GPIO10
SSD_SR_EN_L	P2	DEVSLP0/GPIO33
AP_S0IX_WAKE_SEL	C4	SDIO_POWER_EN/GPIO70
SSD_RESET_L	L2	DEVSLP1/GPIO38
CAM_PCIE_RESET_L	N5	DEVSLP2/GPIO39
PCH_TCO_TIMER_DISABLE	V2	SPKR/GPIO81 (IPD PLTRST#)

CPU/MISC

THERMTRIP*	D60	PM_THRMTRIP_L
RCIN*/GPIO82	V4	TBT_CIO_PLUG_EVENT_L
SERIRQ	T4	LPC_SERIRQ
PCH_OPI_COMP	AW15	PCH_OPI_COMP
RSVD	AF20	NC
RSVD	AB21	NC

GPIO / LPIO

GSPI0_CS*/GPIO83	R6	AUD_SPI_CS_L
GSPI0_CLK/GPIO84	L6	AUD_SPI_CLK
GSPI0_MISO/GPIO85 (IPD)	N6	AUD_SPI_MISO
GSPI0_MOSI/GPIO86 (IPD PLTRST#)	L8	AUD_SPI_MOSI
GSPI1_CS*/GPIO87	R7	TPAD_SPI_CS_L
GSPI1_CLK/GPIO88	L5	TPAD_SPI_CLK
GSPI1_MISO/GPIO89 (IPD)	N7	TPAD_SPI_MISO
GSPI_MOSI/GPIO90	K2	TPAD_SPI_MOSI
UART0_RXD/GPIO91	J1	PCH_BT_UART_D2R
UART0_TXD/GPIO92	K3	PCH_BT_UART_R2D
UART0_RTS*/GPIO93	J2	PCH_BT_UART_RTS_L
UART0_CTS*/GPIO94	G1	PCH_BT_UART_CTS_L
UART1_RXD/GPIO0	K4	PCH_UART1_RXD
UART1_TXD/GPIO1	G2	PCH_UART1_TXD
UART1_RST*/GPIO2	J3	JTAG_ISP_TDO
UART1_CTS*/GPIO3	J4	PCH_UART1_CTS_L
I2C0_SDA/GPIO4	F2	AP_S0IX_WAKE_L
I2C0_SCL/GPIO5	F3	AP_RESET_L
I2C1_SDA/GPIO6	G4	PCH_I2C1_SDA
I2C1_SCL/GPIO7	F1	PCH_I2C1_SCL
SDIO_CLK/GPIO64	E3	TBT_POC_RESET_L
SDIO_CMD/GPIO65	F4	BT_PWRRST_L
SDIO_D0/GPIO66 (IPD PLTRST#)	D3	PCH_STRP_TOPBLK_SWP_L
SDIO_D1/GPIO67	E4	ENET_MEDIA_SENSE
SDIO_D2/GPIO68	C3	LCD_IRQ_L
SDIO_D3/GPIO69	E2	LCD_PSR_EN

PP1V05_S0

R1650 1K 5% 1/20W MF 201

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

PLACE NEAR=U0500 AW15 2 54mm
R1655 49.9 1% 1/20W MF 201

PLT_RESET_L

R1621 100K 5% 1/20W MF 201

TPAD_SPI_INT_GPIO28_L

R1681 0 5% 1/20W MF 0201

TPAD_SPI_INT_L

R1682 0 5% 1/20W MF 0201

TPAD_SPI_INT_GPIO46_L

R1639 100K 5% 1/20W MF 201

R1680 100K 5% 1/20W MF 201

PP3V3_S0

R1641 1K 5% 1/20W MF 201

PLT_RESET_L

R1671 100K 5% 1/20W MF 201

Pull-up on TBT page

Requires connection to SMC via 1K series R

PP3V3_S5
PP3V3_S3
PP3V3_S3
PP3V3_S3
PP3V3_S3RS0_CAMERA
PP3V3_S0
PP3V3_S0

TBTLC for CR, S0 for RR

R1610	100K	XDP_PCH_GPIO76	
R1614	100K	XDP_LPCPLUS_GPIO	
R1615	100K	XDP_PCH_GPIO17	
SD_ON_MLB			
R1616	100K	SD_RESET_L	R1616 should also be stuffed if platform does not use SD card
R1617	100K	SMC_WAKE_SCI_L	
R1618	100K	TPAD_SPI_INT_L	
R1619	100K	TPAD_USB_IF_EN	
R1620	100K	SSD_PWR_EN	SSD_LPSR:S0 BOM option is on R1620
SSD_LPSR:S0			
R1622	100K	HDD_PWR_EN	
R1623	100K	XDP_SDCONN_STATE_CHANGE_L	
R1624	100K	SD_PWR_EN	
R1625	100K	TBT_PWR_EN	
R1626	100K	XDP_JTAG_ISP_TCK	
R1627	100K	XDP_JTAG_ISP_TDI	
R1628	100K	JTAG_TBT_TMS_PCH	
R1629	100K	PCH_HSIO_PWR_EN	
R1630	100K	TPAD_SPI_IF_EN	
R1632	100K	SPIROM_USE_MLB	Stuffed R1632
R1633	100K	CAMERA_PWR_EN_PCH	
R1634	100K	TPAD_SPI_INT_GPIO46_L	No-Stuffed R1634
NOSTUFF			
R1637	100K	SSD_SR_EN_L	
R1638	100K	AP_S0IX_WAKE_SEL	
R1640	100K	XDP_FW_PME_L	
R1652	10K	LPC_SERIRQ	
R1691	100K	BT_PWRRST_L	
R1693	100K	ENET_MEDIA_SENSE	
R1694	100K	LCD_IRQ_L	
R1695	100K	LCD_PSR_EN	

PP3V3_S0

AUD_SPI_CS_L	R1660	100K	
AUD_SPI_CLK	R1661	100K	
AUD_SPI_MISO	R1662	100K	
AUD_SPI_MOSI	R1663	100K	
TPAD_SPI_CS_L	R1664	47K	
TPAD_SPI_CLK	R1665	47K	
TPAD_SPI_MISO	R1666	47K	
TPAD_SPI_MOSI	R1667	47K	
PCH_BT_UART_D2R	R1668	47K	
PCH_BT_UART_R2D	R1669	47K	
PCH_UART1_RXD	R1672	47K	
PCH_UART1_TXD	R1673	47K	
JTAG_ISP_TDO	R1674	100K	
PCH_UART1_CTS_L	R1675	47K	
AP_S0IX_WAKE_L	R1676	100K	
PCH_I2C1_SDA	R1678	2.2K	
PCH_I2C1_SCL	R1679	2.2K	
PCH_BT_UART_RTS_L	R1670	47K	
PCH_BT_UART_CTS_L	R1677	47K	

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Merged (CPU/PCH) Micro2-XDP

Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

(TP P6)

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals		Non-XDP Signals
XDP_MLB_RAMCFG0	TP1870	
XDP_USB_EXTA_OC_L	TP1871	XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	TP1872	XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	TP1873	
XDP_USB_EXTD_OC_L	TP1874	
XDP_SDCONN_STATE_CHANGE_L	TP1875	XDP_SDCONN_STATE_CHANGE_L
XDP_MLB_RAMCFG1	TP1876	
XDP_MLB_RAMCFG2	TP1877	
XDP_MLB_RAMCFG3	TP1878	
XDP_JTAG_ISP_TCK		XDP_JTAG_ISP_TCK
XDP_FW_PME_L	TP1879	
XDP_PCH_GPIO35	TP1880	
XDP_PCH_UART_SSD_L_BT_H	TP1881	
XDP_SSD_PCIE0_SEL_L	R1884 1K	
XDP_LPCPLUS_GPIO		XDP_LPCPLUS_GPIO
XDP_PCH_GPIO17	TP1886	
XDP_PCH_GPIO76	TP1887	
XDP_JTAG_ISP_TDI		XDP_JTAG_ISP_TDI

Unused & MLB_RAMCFGx GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.

SSD_PCIEx_SEL_L straps are connected via 1K to common net.

LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

CPU JTAG Isolation

PP5V_S0, PP3V3_S5 → C1845 0.1UF → U1845 74LVC1G07GF (SOT891) VCC/GND
R1845 330K: ALL_SYS_PWRGD → XDP_JTAG_CPU_ISOL_L
NC ×, NC ×

Merged (CPU/PCH) Micro2-XDP

PP1V05_S0 → R1830 150 → XDP_PRESENT#

CRITICAL XDP_CONN J1800 DF40RC-60DP-0.4V M ST SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to support chipset debug.

	J1800		J1800	
XDP_CPU_PREQ_L	OBSEN_A0	CPU_CFG<17>	OBSEN_C0	
XDP_CPU_PRDY_L	OBSEN_A1	CPU_CFG<16>	OBSEN_C1	
CPU_CFG<0>	OBSDATA_A0	CPU_CFG<8>	OBSDATA_C0	
CPU_CFG<1>	OBSDATA_A1	CPU_CFG<9>	OBSDATA_C1	
CPU_CFG<2>	OBSDATA_A2	CPU_CFG<10>	OBSDATA_C2	
CPU_CFG<3>	OBSDATA_A3	CPU_CFG<11>	OBSDATA_C3	
XDP_BPM_L<0>	OBSEN_B0	CPU_CFG<19>	OBSEN_D0	
XDP_BPM_L<1>	OBSEN_B1	CPU_CFG<18>	OBSEN_D1	
CPU_CFG<4>	OBSDATA_B0	CPU_CFG<12>	OBSDATA_D0	
CPU_CFG<5>	OBSDATA_B1	CPU_CFG<13>	OBSDATA_D1	
CPU_CFG<6>	OBSDATA_B2	CPU_CFG<14>	OBSDATA_D2	
CPU_CFG<7>	OBSDATA_B3	CPU_CFG<15>	OBSDATA_D3	
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC	
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC	
	VCC_OBS_AB	VCC_OBS_CD		
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L	
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L	
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO	
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L	
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI	
	TCK0	TMS	XDP_PCH_TMS	

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_CPU_PRESENT_L

C1804 0.1UF 10% 6.3V CERM X5R 0201
R1831 1K 5% 1/16W MF LF 402
C1800 0.1UF 10% 6.3V CERM X5R 0201
C1801 0.1UF 10% 6.3V CERM X5R 0201
C1806 0.1UF 10% 6.3V CERM X5R 0201

518S0847

CPU_VCCST_PWRGD → R1800 1K (PLACE NEAR=U0500 C61 2 54mm)
PM_PWRBTN_L → R1802 0 (PLACE NEAR=U0500 J3 2 54mm)
PM_PCH_SYS_PWROK → R1804 0 (5% 1/16W MF LF 402)
XDP_CPU_TCK
PCH_JTAGX → R1835 0 (5% 1/20W MF 0201 PLACE NEAR=J1800 58 28mm)

R1805 1K: XDP_CPURST_L → PLT_RESET_L (PLACE NEAR=U0500 AG7 2 54mm)

XDP_CPU_TDO → R1810 51 (PLACE NEAR=U0500 F62 28mm)
XDP_CPU_TCK → R1813 51 (PLACE NEAR=U0500 E60 28mm)
TDI and TMS are terminated in CPU.

CRITICAL Q1840 DMN5L06VK-7 SOT563 — XDP_CPU_TDO (PLACE NEAR=J1800 51 28MM)
CRITICAL Q1840 DMN5L06VK-7 SOT563 — XDP_CPUPCH_TRST_L (MAKE BASE=TRUE) → XDP_CPUPCH_TRST_L
CRITICAL Q1842 DMN5L06VK-7 SOT563 — XDP_CPU_TDI (PLACE NEAR=J1800 55 28mm)
CRITICAL Q1842 DMN5L06VK-7 SOT563 — XDP_CPU_TMS

PP1V05_SUS

PCH_JTAGX	R1899 1K	NO STUFF
XDP_PCH_TDO	R1890 51	XDP
XDP_PCH_TDI	R1891 51	XDP
XDP_PCH_TMS	R1892 51	XDP
XDP_PCH_TCK	R1896 51	NO STUFF
XDP_CPUPCH_TRST_L	R1897 51	NO STUFF

(5% 1/20W MF 201)

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System RTC Power Source & 32kHz / 25MHz Clock Generator

Chipset uses 24MHz crystal, GreenCLK kept to save 1x 25MHz crystal & 1x 32kHz crystal

This looks a little ugly to support
new and old parts. With GreenCLK Rev C
pin 5 must receive S5 power (Stuff R2042)

PP3V42_G3H
Coin-Cell: VBAT (300-ohm & 10uF RC)
No Coin-Cell: 3.42V G3Hot (no RC)

PP3V3_S5
Coin-Cell & G3Hot: 3.42V G3Hot
Coin-Cell & No G3Hot: 3.3V S5
No Coin-Cell: 3.3V S5
No bypass necessary

GreenCLK 25MHz Power — PP3V3_S5RS3RS0_SYSCLKGEN
Must be powered if any VDDIO is powered.

CAM XTAL Power
TBT XTAL Power — PP1V2_CAM_XTALPCIEVDD, PP3V3_TBTLC

VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.

+V3.3A should be first available ~3.3V power to reduce VBAT draw.

U1900 SLG3NB148CV TQFN CRITICAL

C1924 0.1UF 10% 16V X5R CERM 0201
C1922 0.1UF 10% 16V X5R CERM 0201
C1902 1UF 20% 6.3V X5R 0201

CKPLUS WAIVE=PwrTerm2Gnd

C1905 12PF 5% 25V NP0 C0G CERM 0201
C1906 12PF 5% 25V NP0 C0G CERM 0201
Y1905 CRITICAL 25.000MHZ-12PF-20PPM SM 3 2X2 5MM
R1905 0 5% 1/20W MF 0201 — NO STUFF
R1906 1M 5% 1/20W MF 201

SYSCLK CLK25M X2 → SYSCLK CLK25M X2 R → X2
SYSCLK CLK25M X1 ← X1

NOTE: 30 PPM or better required for RTC accuracy

32.768K → PCH CLK32K RTCX1 (OUT)
SYSCLK CLK25M CAMERA (OUT)
SYSCLK CLK25M TBT (OUT)
PPVRTC G3H (OUT) — For SB RTC Power
C1910 1UF 20% 6.3V X5R 0201

NC_RTC_CLK32K_RTCX2 (MAKE BASE=TRUE) — NC_RTC_CLK32K_RTCX2 (NO TEST=TRUE)

PCH Reset Button

PP3V3_S0
R1995 10K 5% 1/20W MF 201
XDP
R1996 0 1/20W 0201 MF 5%
XDP_DBRESET_L → PM_SYSRST_L
NO STUFF
R1997 0 5% 1/16W MF 402
SILK PART=SYS RESET

Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).

PP1V2_S3
PP3V3_S0
C1970 0.1UF 10% 16V X5R CERM 0201
U1970 74AUP1G07GF SOT891
R1970 330K 5% 1/20W MF 201
TPS51916 I(leak) = +/- 1uA, Vih(min) = 1.8V
33uW when driven-low
CPU_MEMVTT_PWR_EN_LSVDDQ
MEMVTT_PWR_EN (MAKE BASE=TRUE) → MEMVTT_PWR_EN (OUT)

PCH ME Disable Strap

PP5V_S0
R1920 100K 5% 1/20W MF 201
Q1920 DMN5L06VK-7 SOT563 VER 3
SPI_DESCRIPTOR_OVERRIDE_LS5V
PP1V5_S0SW_AUDIO_HDA
SPI_DESCRIPTOR_OVERRIDE
R1921 1K 5% 1/20W MF 201
HDA_SDOUT_R (OUT) — IPD = 9-50k
SPI_DESCRIPTOR_OVERRIDE_L

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

PCH 24MHz Crystal

C1915 6.8PF +/- 0.1PF 25V C0G 0201
C1916 6.8PF +/- 0.1PF 25V C0G 0201
Y1915 CRITICAL 24.000MHZ-20PPM-6PF 3 20X2 50MM SM1
R1915 0 5% 1/20W MF 0201
PCH_CLK24M_XTALOUT_R → PCH_CLK24M_XTALOUT (IN)
R1916 1M 5% 1/20W MF 201
PCH_CLK24M_XTALIN (OUT)

PCH 24MHz Outputs

R1927 22 5% 1/20W MF 201
LPC_CLK24M_SMC_R — PLACE NEAR=U0500 AN15 5 1mm
LPC_CLK24M_SMC (MAKE BASE=TRUE) → LPC_CLK24M_SMC (OUT)

VCCST (1.05V S0) PWRGD

PP3V3_S5
C1930 0.1UF 10% 16V X5R CERM 0201
U1930 CRITICAL 74AUP1G09 SOT891
PP1V05_S0
R1931 10K 5% 1/20W MF 201
ALL_SYS_PWRGD
PM_SLP_S3_L
CPU_VCCST_PWRGD (OUT)

PCH PWROK Generation

PP3V42_G3H
PP3V3_S0
C1950 0.1UF 10% 16V X5R CERM 0201 BYPASS=U1950 5MM
R1950 10K 5% 1/20W MF 201
CPU_VR_EN
R1955 10K 5% 1/20W MF 201
NO STUFF R1951 0 5% 1/20W MF 0201
CPU_VR_READY (MAKE BASE=TRUE) → CPU_VR_READY (IN)
ALL_SYS_PWRGD
CPUVR_PGOOD_R
U1950 74LVC2G08GT SOT833
PM_S0_PGOOD
R1963 0 5% 1/20W MF 0201
NO STUFF R1960 0 5% 1/20W MF 0201 — WF: Do we need this?
CKPLUS WAIVE=UNCONNECTED PINS
NO STUFF R1961 100K 5% 1/20W MF 201
SYS_PWROK_R
R1962 1K 5% 1/20W MF 201
PM_PCH_PWROK (MAKE BASE=TRUE) → PM_PCH_PWROK (OUT)
PM_PCH_SYS_PWROK (OUT)
SMC_DELAYED_PWRGD

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Platform Reset Connections

Unbuffered

PLT_RESET_L

R2071 0 5% 1/20W MF 0201

PCA9557D_RESET_L

Scrub for Layout Optimization

Buffered

PP3V3_S0

CRITICAL
MC74VHC1G08 SC70 HF
U2071

C2071 0.1UF 10% 16V X5R CERM 0201

R2070 100K 5% 1/20W MF 201

PLT_RST_BUF_L

R2072 0 5% 1/20W MF 0201

SMC_LRESET_L

R2088 0 5% 1/20W MF 0201

BKLT_PLT_RST_L

NOSTUFF
R2089 0 5% 1/20W MF 0201

CAM_PCIE_RESET_L

PCH_TBT_PCIE_RESET_L
MAKE BASE=TRUE

PCH_TBT_PCIE_RESET_L

PP3V3_S5

NOSTUFF
BYPASS=U2030 3mm
C2030 0.1UF 10% 10V X5R CERM 0201

NOSTUFF
CRITICAL
74LVC1G08 SOT891
U2030 08

PM_SLP_S4_L

CAMERA_PWR_EN_PCH

CAMERA_PWR_EN

NC

R2030 0 5% 1/20W MF 0201

Power State Debug LEDs

(For development only)

DBGLED

PP3V3_S5

R2094 0 5% 1/16W MF LF 402

PLACE SIDE=BOTTOM

PP3V3_S5_DBGLED
MIN LINE WIDTH=0.5 MM
MIN NECK WIDTH=0.25 MM
VOLTAGE=3.3V

R	Net	D	Q	Signal
R2090 20K	DBGLED_S5	D2090 GREEN 56MCD 2MA 2.65V LTQH9G SM, PLACE SIDE=BOTTOM, SILK PART=S5 ON		
R2091 20K	DBGLED_S4	D2091 GREEN 56MCD 2MA 2.65V LTQH9G SM, PLACE SIDE=BOTTOM, SILK PART=STBY ON	DBGLED_S4_D	Q2090 DMN5L06VK-7 SOT563 VER 3
R2092 20K	DBGLED_S3	D2092 GREEN 56MCD 2MA 2.65V LTQH9G SM, PLACE SIDE=BOTTOM, SILK PART=S3 ON	DBGLED_S3_D	Q2090 DMN5L06VK-7 SOT563 VER 3
R2093 20K	DBGLED_S0I3	D2093 GREEN 56MCD 2MA 2.65V LTQH9G SM, PLACE SIDE=BOTTOM, SILK PART=S0I3 ON	DBGLED_S0I3_D	Q2091 DMN5L06VK-7 SOT563 VER 3
R2095 20K	DBGLED_S0	D2095 GREEN 56MCD 2MA 2.65V LTQH9G SM, PLACE SIDE=BOTTOM, SILK PART=S0 ON	DBGLED_S0_D	Q2091 DMN5L06VK-7 SOT563 VER 3

S4_PWR_EN
PM_SLP_S4_L
PM_SLP_S3_L
PM_SLP_S0_L

GreenCLK 25MHz Power

PP3V3_S3

NO STUFF
R2040 0 5% 1/20W MF 0201

PP3V3_S5R3RS0_SYSCLKGEN

PP3V3_S5R3RS0_SYSCLKGEN
MIN LINE WIDTH=0.5 MM
MIN NECK WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE BASE=TRUE

PP3V3_S0

NO STUFF
R2041 0 5% 1/20W MF 0201

R2041/2 should be stuffed for GreekCLK A or B depending on S2 rail

R2042 should be stuffed for GreenCLK C

PP3V3_S5

R2042 0 5% 1/20W MF 0201

Redwood Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH

PP3V3_TBTLC

R2061 100K 5% 1/20W MF 201

C2060 0.1UF 20% 10V CERM 402

R2062 100K 5% 1/20W MF 201

U2060 74LVC2G07 SOT891 (VCC, GND)

From RR

From PCH

JTAG_TBT_TDO

JTAG_TBT_TMS_PCH

S0 pull-up on PCH page

S0 pull-up on PCH page

JTAG_ISP_TDO

JTAG_TBT_TMS

To PCH

To RR

NOTE: Solution shown is for LPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.

NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary.

Pin N61 needs a TP for Power to perform iFDIM test
Renaming the pins N61 and P61 to remove automatic diffpari property

TP_CPU_RSVDN61 — TP_CPU_RSVDN61 (MAKE BASE=TRUE)

TP_CPU_RSVDP61 — TP_CPU_RSVDP61 (MAKE BASE=TRUE)

RAM Configuration Straps

Pull-downs for chip-down RAM systems

XDP_MLB_RAMCFG0
XDP_MLB_RAMCFG1
XDP_MLB_RAMCFG2
XDP_MLB_RAMCFG3

	RAMCFG3:L	RAMCFG2:L	RAMCFG1:L	RAMCFG0:L
	R2050 10K	R2051 10K	R2052 10K	R2053 10K

LPDDR3 Alias Support

TP_CPU_MEM_RESET_L — TP_CPU_MEM_RESET_L (MAKE BASE=TRUE)

TP_MEM_VDD_SEL_1V5_L — TP_MEM_VDD_SEL_1V5_L (MAKE BASE=TRUE)

PP0V6_S3_MEM_VREFDQ_A — PP0V6_S3_MEM_VREFDQ_A (MAKE BASE=TRUE, VOLTAGE=0.6V)

PP0V6_S3_MEM_VREFCA_A — PP0V6_S3_MEM_VREFCA_A (MAKE BASE=TRUE, VOLTAGE=0.6V)

PP0V6_S3_MEM_VREFDQ_B — PP0V6_S3_MEM_VREFDQ_B (MAKE BASE=TRUE, VOLTAGE=0.6V)

PP0V6_S3_MEM_VREFCA_B — PP0V6_S3_MEM_VREFCA_B (MAKE BASE=TRUE, VOLTAGE=0.6V)

DDC Pull-Ups

2.2k pull-ups are required by PCH
to indicate active display interface.

DP++ spec violation, should remove!

PP3V3_S0

NO STUFF
R2020 2.2K 5% 1/20W MF 201

R2021 2.2K 5% 1/20W MF 201

NO STUFF
R2022 2.2K 5% 1/20W MF 201

R2023 2.2K 5% 1/20W MF 201

DP_TBTSNK0_DDC_CLK
DP_TBTSNK0_DDC_DATA
DP_TBTSNK1_DDC_CLK
DP_TBTSNK1_DDC_DATA

TBTSNK1_DDC is pulled-up just to indicate that DP port is used. No DDC on this port, AUX-only.

NOTE: Only DDC_DATA is sensed by PCH, so DDC_CLK pull-ups are unstuffed.

Thunderbolt Pull-up/downs

PP3V3_S0

CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC (on TBT page)

R2015 100K 5% 1/20W MF 201

Falcon Ridge PLUG_EVENT is active-low, always driven (pull-up)

TBT_CIO_PLUG_EVENT_L — MAKE BASE=TRUE — TBT_CIO_PLUG_EVENT_L

Required for unused second TBT port

TBT_B_CIO_SEL
DP_TBTPB_HPD
TBT_B_CONFIG2_RC
TBT_B_CONFIG1_BUF
TBT_B_LSRX

R2016 10K 5% 1/20W MF 201

R2017 10K 5% 1/20W MF 201

R2018 10K 5% 1/20W MF 201

R2019 10K 5% 1/20W MF 201

R2014 10K 5% 1/20W MF 201

TBT Aliases

MAKE BASE=TRUE

DP_TBTSNK0_DDC_CLK — DP_TBTSNK0_DDC_CLK
DP_TBTSNK0_DDC_DATA — DP_TBTSNK0_DDC_DATA

MAKE BASE=TRUE

DP_TBTSNK1_HPD — DP_TBTSNK1_HPD
=DP_TBTSNK1_ML_C_P<3..0> — =DP_TBTSNK1_ML_C_P<3..0>
=DP_TBTSNK1_ML_C_N<3..0> — =DP_TBTSNK1_ML_C_N<3..0>
DP_TBTSNK1_AUXCH_C_P — DP_TBTSNK1_AUXCH_C_P
DP_TBTSNK1_AUXCH_C_N — DP_TBTSNK1_AUXCH_C_N
DP_TBTSNK1_DDC_CLK — DP_TBTSNK1_DDC_CLK
DP_TBTSNK1_DDC_DATA — DP_TBTSNK1_DDC_DATA

Single-port TBT implementation does not require DDC Crossbar

XDP_JTAG_ISP_TCK — XDP_JTAG_ISP_TCK
XDP_JTAG_ISP_TDI — XDP_JTAG_ISP_TDI

No MAKE_BASE on TCK/TDI as these are provided on XDP page.

PP3V3_SUS

R2010 100K 5% 1/20W MF 201

PCH_SML1ALERT_L

SYNC_MASTER=J43_MLB	SYNC_DATE=01/17/2013
PAGE TITLE	Project Chipset Support
	Apple Inc.
DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
PAGE	20 OF 120
SHEET	18 OF 73

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Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

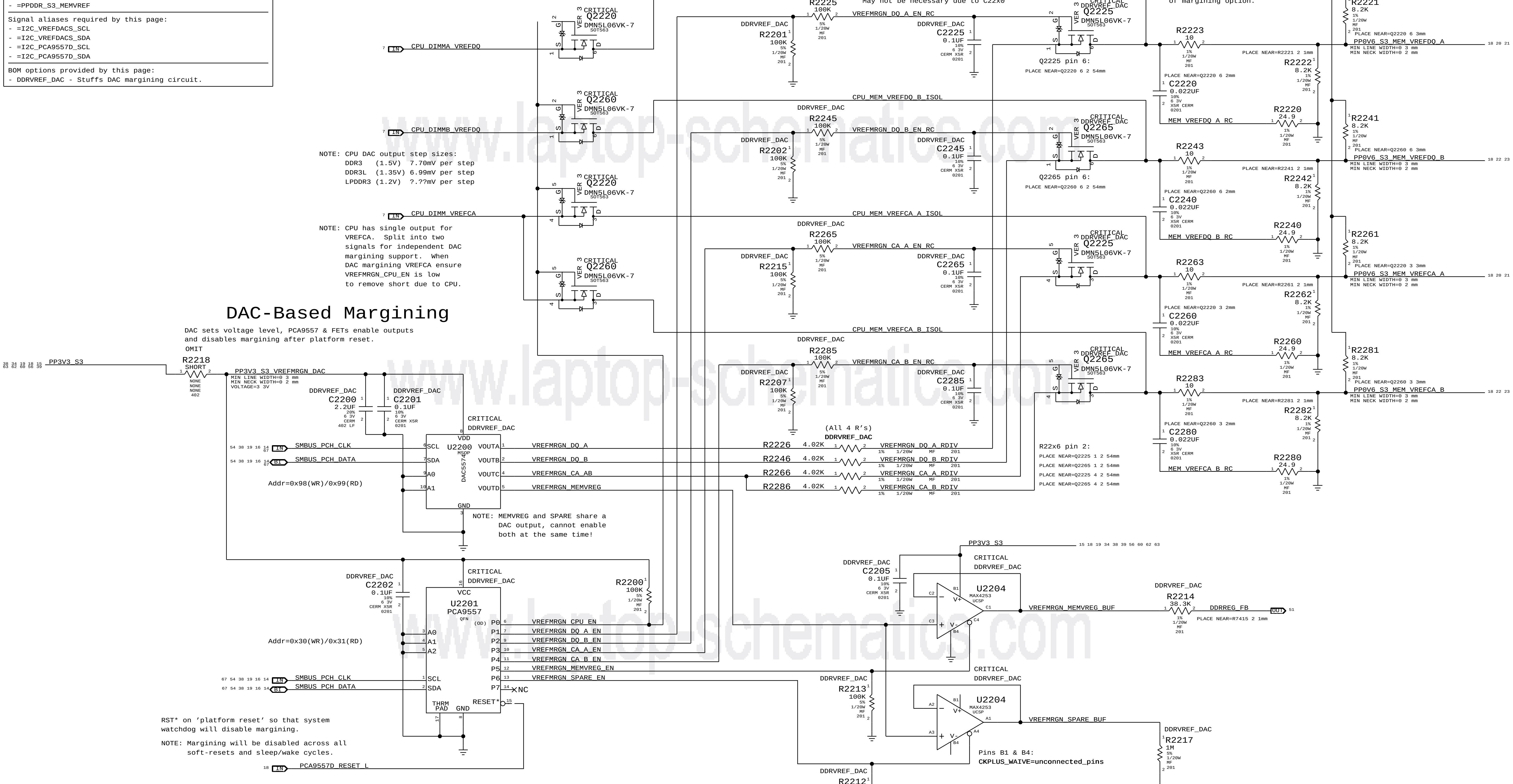
FETs for CPU isolation during DAC margining

VRef Dividers

Always used, regardless of margining option.

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.



	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG
DAC Channel:	A	B	C	C	D
PCA9557D Pin:	1	2	3	4	5

	LPDDR3 (1.2V)	DDR3L (1.35V)	LPDDR3 (1.2V)	DDR3L (1.35V)
Nominal value	0.600V (DAC: 0x2E.5)	0.675V (DAC: 0x34)	1.200V (DAC: 0x5D)	1.343V (DAC: 0x68)
Margined target:	0.300V - 0.900V (+/- 300mV)	0.337V - 1.013V (+/- 337.5mV)	0.800V - 1.600V (+/- 400mV)	0.972V - 1.714V (+/- 371mV)
DAC range:	0.000V - 1.199V (0x00 - 0x5D)	0.000V - 1.354V (0x00 - 0x69)	0.000V - 2.397V (0x00 - 0xBA)	0.000V - 2.694V (0x00 - 0xD1)
VRef current:	+73uA - -73uA (- = sourced)	+82uA - -82uA (- = sourced)	+21uA - -21uA (- = sourced)	+25uA - -25uA (- = sourced)
DAC step size:	6.36mV / step @ output	6.36mV / step @ output	4.28mV / step @ output	3.53mV / step @ output

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

SYNC_MASTER=WILL_J43 SYNC_DATE=02/04/2013

PAGE TITLE: DDR3 VREF MARGINING

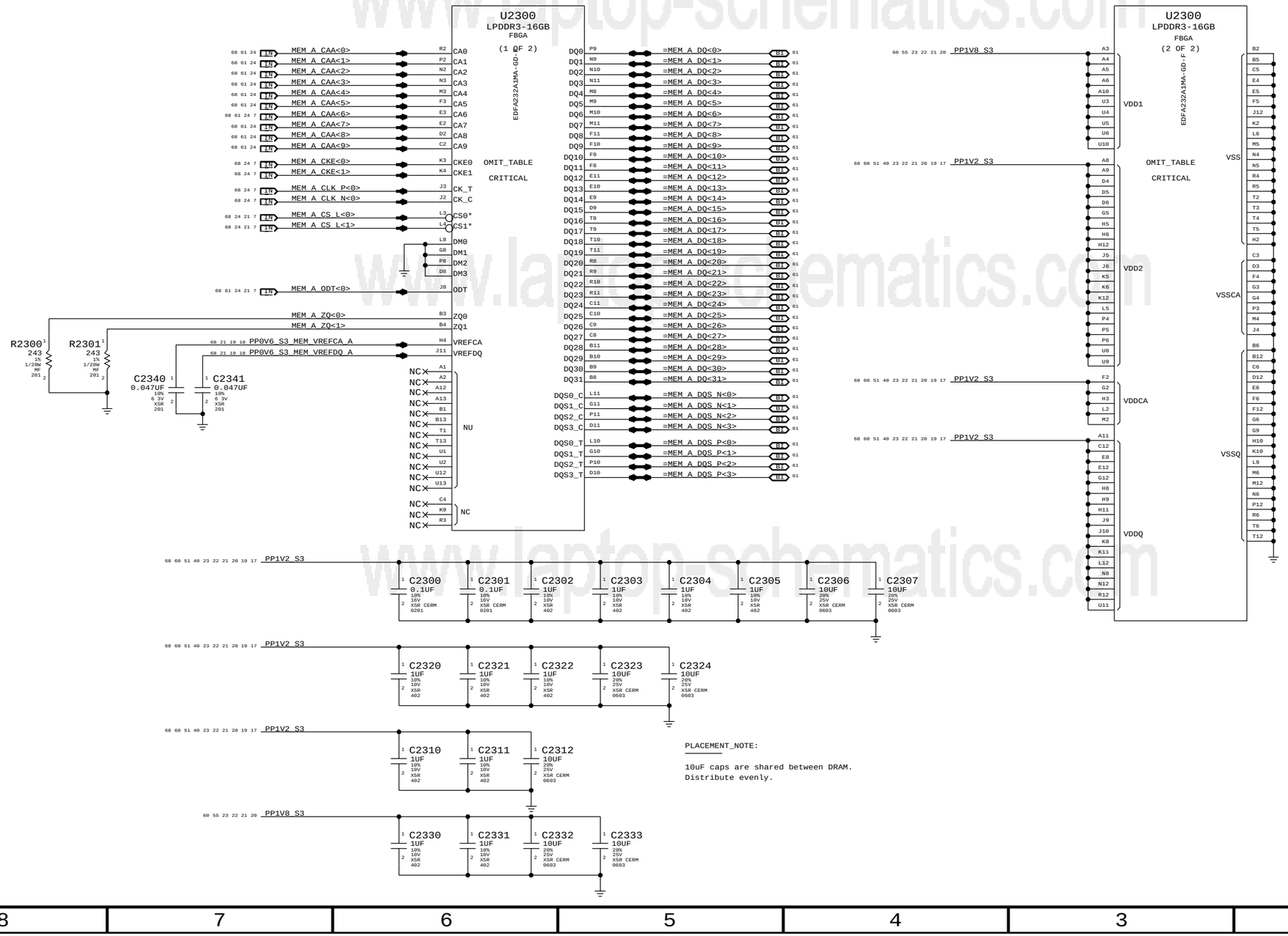
Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

LPDDR3 CHANNEL A (0-31)



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

LPDDR3 DRAM Channel A (0-31)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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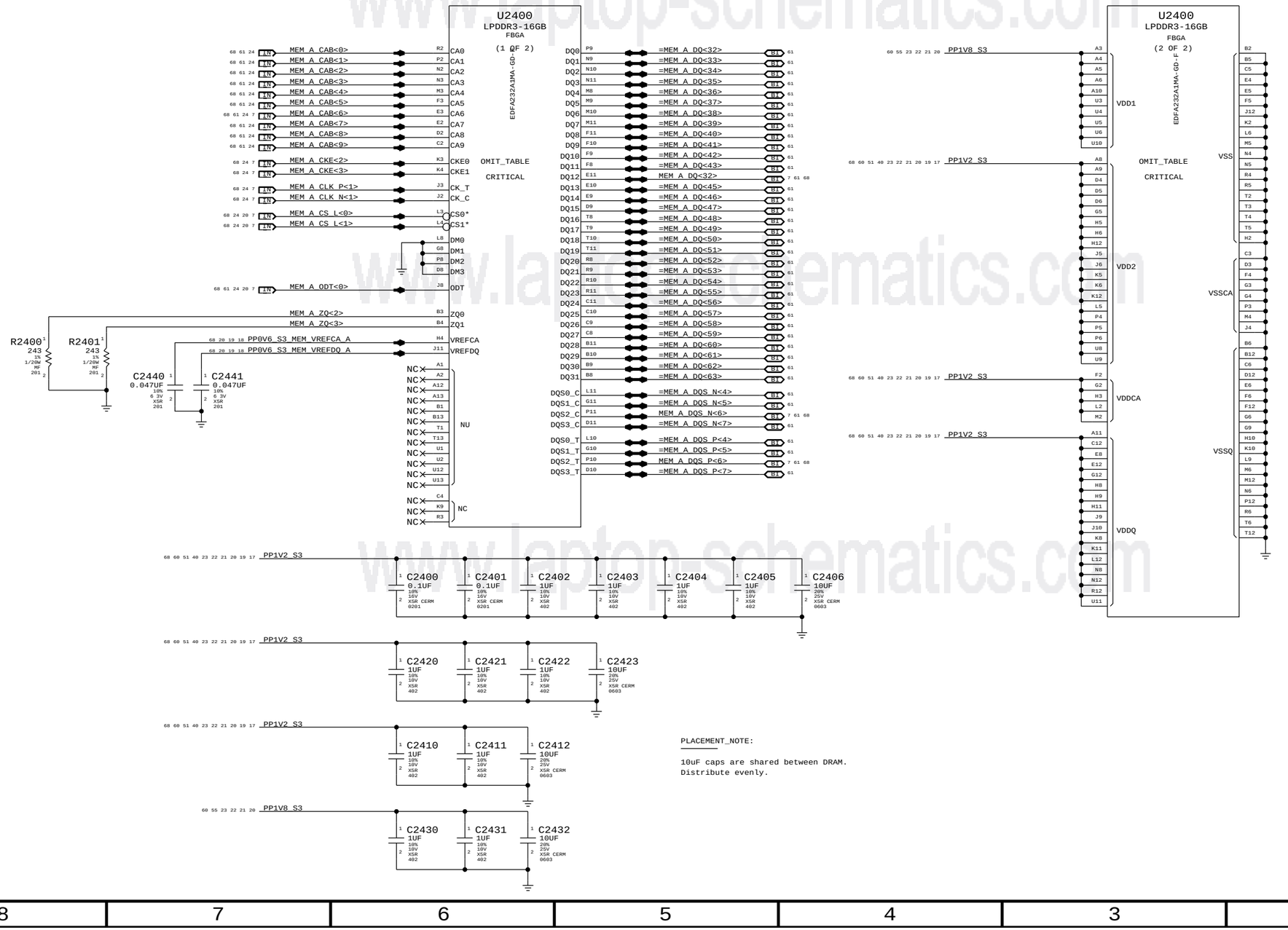
LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: LPDDR3 DRAM Channel A (32-63)

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 24 OF 120

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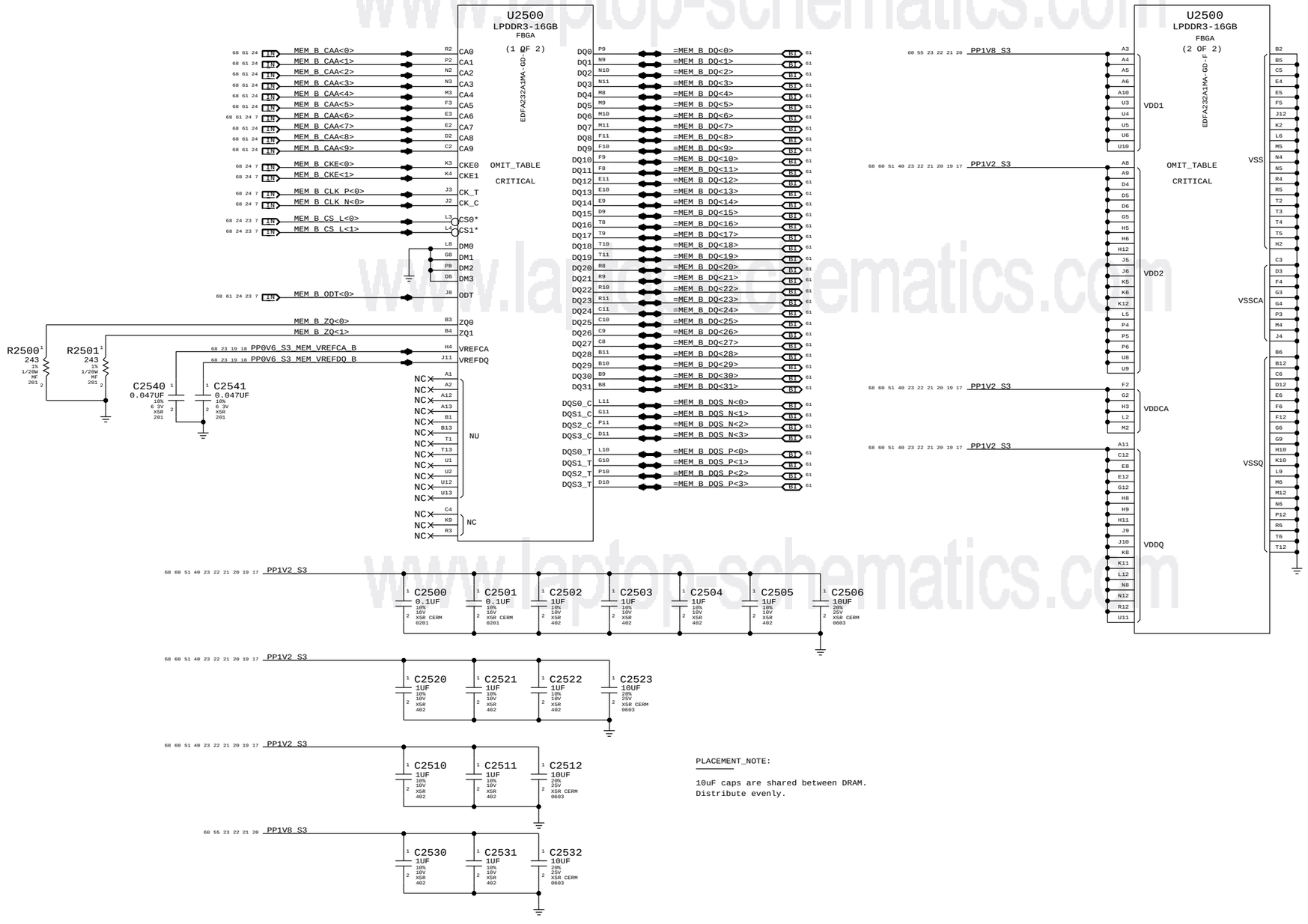
LPDDR3 CHANNEL B (0-31)



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

LPDDR3 DRAM Channel B (0-31)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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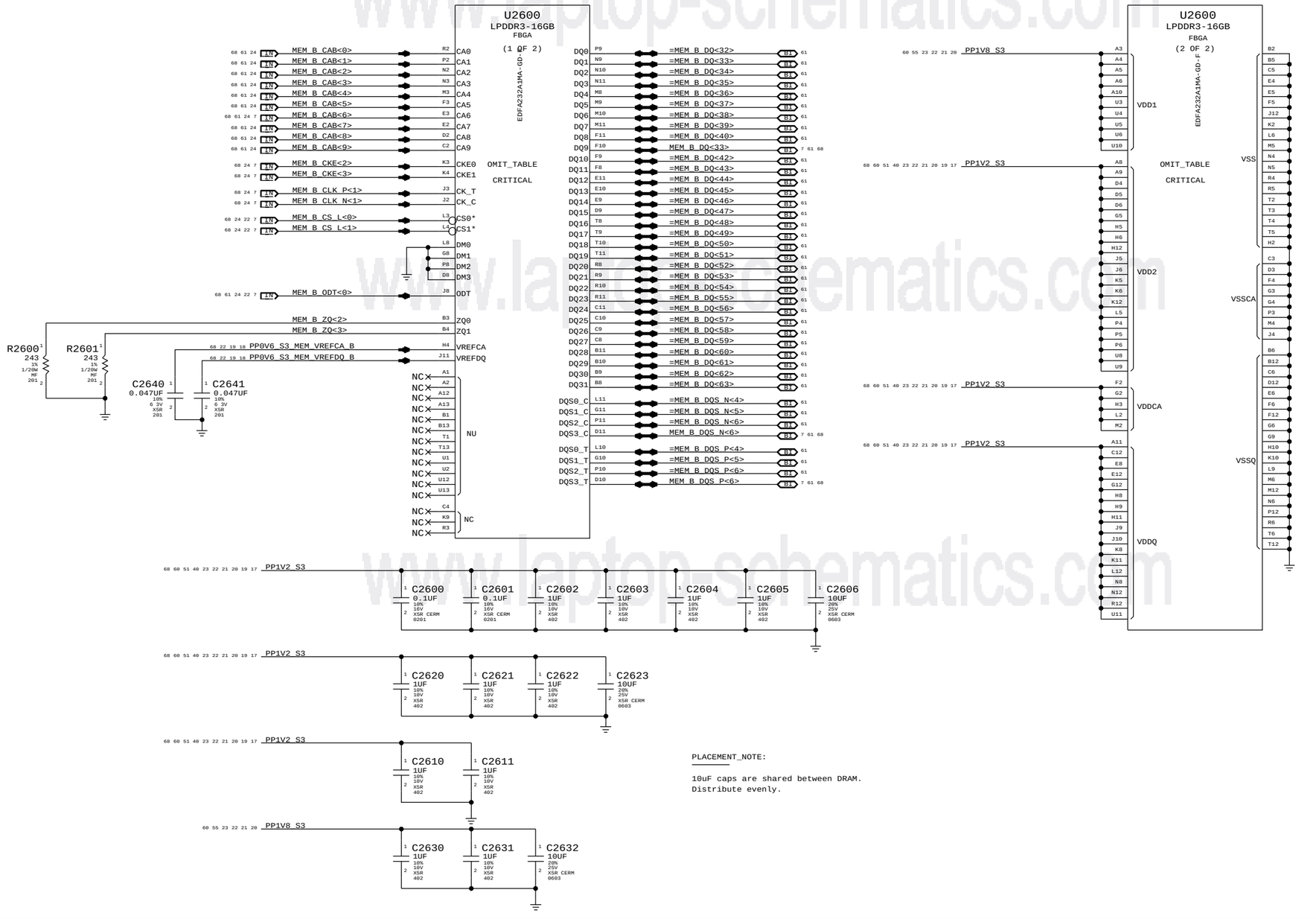
LPDDR3 CHANNEL B (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
LPDDR3 DRAM Channel B (32-63)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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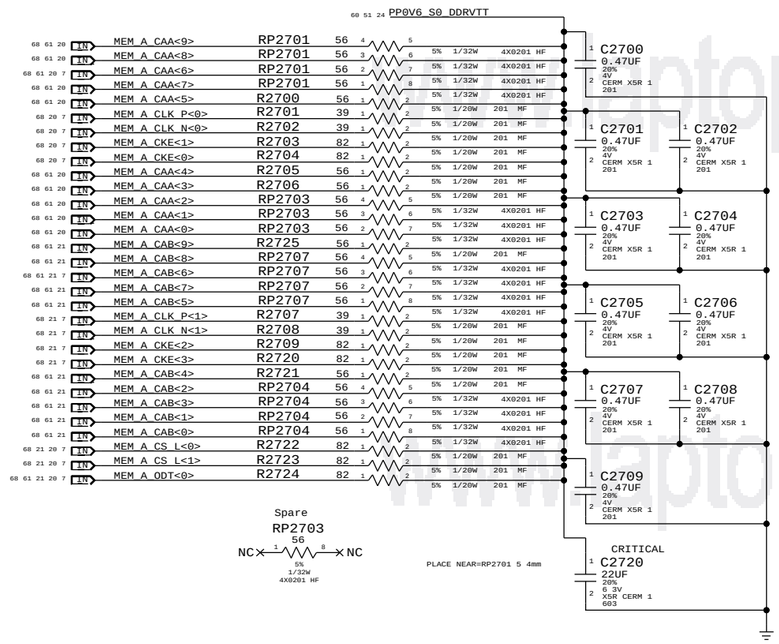
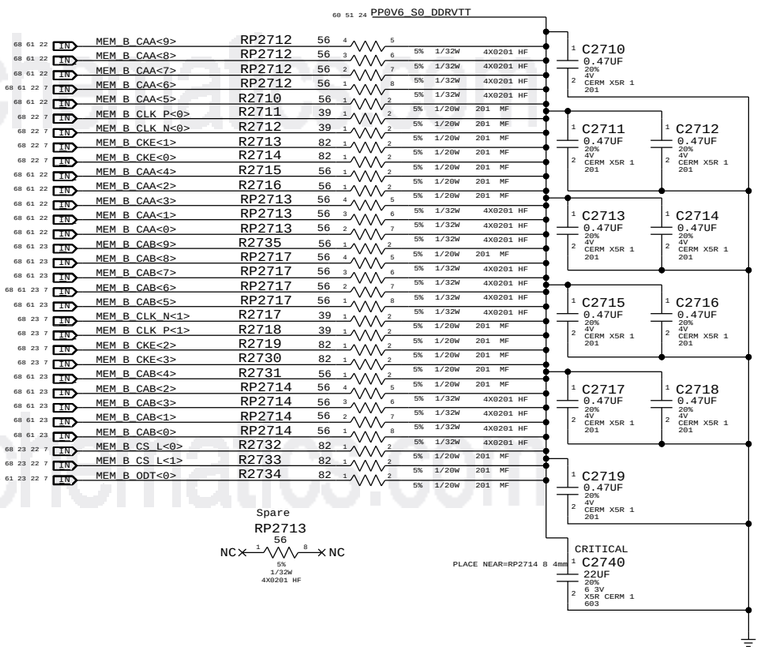
SHEET 23 OF 73

Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





SYNC MASTER=J43_MLB SYNC DATE=09/21/2012

PAGE TITLE

LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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CRITICAL
OMIT_TABLE

U2800
FALCON-RIDGE-FR2C
FCBGA
SYM 1 OF 2

PCIE GEN2

PCIE_TBT_R2D_C_P<0>	C2800 0.1UF	PCIE_TBT_R2D_P<0>	AB9	PERP_0	
PCIE_TBT_R2D_C_N<0>	C2801 0.1UF	PCIE_TBT_R2D_N<0>	AA10	PERN_0	
PCIE_TBT_R2D_C_P<1>	C2802 0.1UF	PCIE_TBT_R2D_P<1>	AA12	PERP_1	
PCIE_TBT_R2D_C_N<1>	C2803 0.1UF	PCIE_TBT_R2D_N<1>	AB13	PERN_1	
PCIE_TBT_R2D_C_P<2>	C2804 0.1UF	PCIE_TBT_R2D_P<2>	AB15	PERP_2	
PCIE_TBT_R2D_C_N<2>	C2805 0.1UF	PCIE_TBT_R2D_N<2>	AA16	PERN_2	
PCIE_TBT_R2D_C_P<3>	C2806 0.1UF	PCIE_TBT_R2D_P<3>	AA18	PERP_3	
PCIE_TBT_R2D_C_N<3>	C2807 0.1UF	PCIE_TBT_R2D_N<3>	AB19	PERN_3	
				PERST_OD_N	
PCH_TBT_PCIE_RESET_L			P5		
TBT_PWR_ON_POC_RST_L			R4	PWR_ON_POC_RSTN	

PCIE_TBT_D2R_C_P<0>	C2840 0.1UF	PCIE_TBT_D2R_P<0>	AD5	PETP_0	
PCIE_TBT_D2R_C_N<0>	C2841 0.1UF	PCIE_TBT_D2R_N<0>	AD7	PETN_0	
PCIE_TBT_D2R_C_P<1>	C2842 0.1UF	PCIE_TBT_D2R_P<1>	AD9	PETP_1	
PCIE_TBT_D2R_C_N<1>	C2843 0.1UF	PCIE_TBT_D2R_N<1>	AD11	PETN_1	
PCIE_TBT_D2R_C_P<2>	C2844 0.1UF	PCIE_TBT_D2R_P<2>	AD13	PETP_2	
PCIE_TBT_D2R_C_N<2>	C2845 0.1UF	PCIE_TBT_D2R_N<2>	AD15	PETN_2	
PCIE_TBT_D2R_C_P<3>	C2846 0.1UF	PCIE_TBT_D2R_P<3>	AD17	PETP_3	
PCIE_TBT_D2R_C_N<3>	C2847 0.1UF	PCIE_TBT_D2R_N<3>	AD19	PETN_3	

MISC

	RSENSE	U20 TBT_RSENSE
R2855 1K 1% 1/20W MF 201	RBIAS	W20 TBT_RBIAS
	RSVD_GND	AD1, L8
	GPIO_16/DEVICE_PCIE_RST_N	W6 TP_TBT_PCIE_RESET0_L
	GPIO_17	AB3 TBT_DFT_STRAP_1
	GPIO_18	AD3 TBT_ROM_SECURITY_XOR
	GPIO_19	V1 TBT_DFT_STRAP_3
	PCIE_CLKREQ_OD_N	V3 TBT_CLKREQ_L
	REFCLK_100_IN_P	AB21 PCIE_CLK100M_TBT_P
	REFCLK_100_IN_N	AD21 PCIE_CLK100M_TBT_N
	XTAL_25_IN	AA24 SYSCLK_CLK25M_TBT_R
	XTAL_25_OUT	AB23 TP_TBT_XTAL25OUT
	TMU_CLK_OUT	AA4 TBT_TMU_CLK_OUT

Used for straps in host mode

Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.

If strap != bit then security is enabled?

Divides 3.3V to 1.8V

R2895 806 1% 1/20W MF 201 — SYSCLK_CLK25M_TBT

NO STUFF R2899 10K 5% 1/20W MF 201

R2896 1K 5% 1/20W MF 201

NO STUFF R2867 10K 5% 1/20W MF 201

R2861 10K 5% 1/20W MF 201 — R2862 10K 5% 1/20W MF 201 — R2863 10K 5% 1/20W MF 201

R2881 100K 5% 1/20W MF 201 — R2880 100K 5% 1/20W MF 201 — R2882 100K 5% 1/20W MF 201

R2878 100K 5% 1/20W MF 201 — R2879 100K 5% 1/20W MF 201

R2832 100K 5% 1/20W MF 201 — R2883 100K 5% 1/20W MF 201

NO STUFF R2884 100K 5% 1/20W MF 201 — NO STUFF R2885 10K 5% 1/20W MF 201 — R2886 10K 5% 1/20W MF 201

R2888 10K 5% 1/20W MF 201 — R2887 10K 5% 1/20W MF 201

DISPLAY PORT

				DPSRC_3_P	A14 TP_DP_TBTSRC_ML_CP<3>
				DPSRC_3_N	B15 TP_DP_TBTSRC_ML_CN<3>
				DPSRC_2_P	A12 TP_DP_TBTSRC_ML_CP<2>
				DPSRC_2_N	B13 TP_DP_TBTSRC_ML_CN<2>
				DPSRC_1_P	A10 NC_DP_TBTSRC_ML_CP<1>
				DPSRC_1_N	B11 NC_DP_TBTSRC_ML_CN<1>
				DPSRC_0_P	A8 TP_DP_TBTSRC_ML_CP<0>
				DPSRC_0_N	B9 TP_DP_TBTSRC_ML_CN<0>
				DPSRC_AUX_P	J4 NC_DP_TBTSRC_AUXCH_CP
				DPSRC_AUX_N	J2 NC_DP_TBTSRC_AUXCH_CN
				DPSRC_HPD_OD	AC2 DP_TBTSRC_HPD
				GPIO_2/TMU_CLK_IN/AC_PRESENT	U2 TBT_GPIO2
				GPIO_3/FORCE_PWR	L6 TBT_PWR_EN
				GPIO_4/WAKE_OD_N	H5 SMC_PME_S4_DARK_L
				GPIO_5/CIO_PLUG_EVENT_N/HV_OK_OD	Y7 TBT_CIO_PLUG_EVENT_L
				GPIO_6_OD/CIO_SDA_OD	Y1 HDMITBTMUX_SEL_TBT
				GPIO_7_OD/CIO_SCL_OD	T7 TBT_GPIO7
				GPIO_8/EN_CIO_PWR_N_OD	V7 TBT_EN_CIO_PWR_L
				GPIO_9/SX_CTRL_OD*	M7 TBT_BATLOW_L
				GPIO_14	T1 TBTDP_AUXIO_EN
				GPIO_15	T3 TBT_DDC_XBAR_EN_L

PORTS

				PA_CIO0_TX_P/DPSRC_0_P	PB_CIO2_TX_P/DPSRC_0_P R24 NC_TBT_B_R2D_CP<0>
				PA_CIO0_TX_N/DPSRC_0_N	PB_CIO2_TX_N/DPSRC_0_N N24 NC_TBT_B_R2D_CN<0>
				PA_CIO0_RX_P	PB_CIO2_RX_P R22 NC_TBT_B_D2RP<0>
				PA_CIO0_RX_N	PB_CIO2_RX_N N22 NC_TBT_B_D2RN<0>
				PA_CONFIG1/CIO_0_LSEO	PB_CONFIG1/CIO_2_LSEO D3 TBT_B_CONFIG1_BUF
				PA_CONFIG2/CIO_0_LSOE	PB_CONFIG2/CIO_2_LSOE M1 TBT_B_CONFIG2_RC
				PA_CIO1_TX_P/DPSRC_2_P	PB_CIO3_TX_P/DPSRC_2_P W24 NC_TBT_B_R2D_CP<1>
				PA_CIO1_TX_N/DPSRC_2_N	PB_CIO3_TX_N/DPSRC_2_N U24 NC_TBT_B_R2D_CN<1>
				PA_CIO1_RX_P	PB_CIO3_RX_P W22 NC_TBT_B_D2RP<1>
				PA_CIO1_RX_N	PB_CIO3_RX_N U22 NC_TBT_B_D2RN<1>
				PA_LSTX/CIO_1_LSEO	PB_LSTX/CIO_3_LSEO M5 NC_TBT_B_LSTX
				PA_LSRX/CIO_1_LSOE	PB_LSRX/CIO_3_LSOE P7 TBT_B_LSRX
				PA_DPSRC_1_P	PB_DPSRC_1_P A20 DP_TBTPB_ML_C_P<1>
				PA_DPSRC_1_N	PB_DPSRC_1_N B21 DP_TBTPB_ML_C_N<1>
				PA_DPSRC_3_P	PB_DPSRC_3_P A22 DP_TBTPB_ML_C_P<3>
				PA_DPSRC_3_N	PB_DPSRC_3_N B23 DP_TBTPB_ML_C_N<3>
				PA_AUX_P	PB_AUX_P K3 NC_DP_TBTPB_AUXCH_CP
				PA_AUX_N	PB_AUX_N K1 NC_DP_TBTPB_AUXCH_CN
				PA_DPSRC_HPD	PB_DPSRC_HPD N6 DP_TBTPB_HPD
				GPIO_0/PA_HV_EN/BYP0	GPIO_1/PB_HV_EN/BYP0 F1 TBT_B_HV_EN
				GPIO_10/PA_CIO_SEL/BYP1	GPIO_11/PB_CIO_SEL/BYP1 R2 TBT_B_CIO_SEL
				GPIO_12/PA_DP_PWRDN/BYP2	GPIO_13/PB_DP_PWRDN/BYP2 F3 TBT_B_DP_PWRDN

				DPSNK0_3_P	DP_TBTSNK0_ML_P<3> E14
				DPSNK0_3_N	DP_TBTSNK0_ML_N<3> D13
				DPSNK0_2_P	DP_TBTSNK0_ML_P<2> E16
				DPSNK0_2_N	DP_TBTSNK0_ML_N<2> D15
				DPSNK0_1_P	DP_TBTSNK0_ML_P<1> E18
				DPSNK0_1_N	DP_TBTSNK0_ML_N<1> D17
				DPSNK0_0_P	DP_TBTSNK0_ML_P<0> E20
				DPSNK0_0_N	DP_TBTSNK0_ML_N<0> D19
				DPSNK0_AUX_P	DP_TBTSNK0_AUXCH_P G4
				DPSNK0_AUX_N	DP_TBTSNK0_AUXCH_N G2
R2830 100K 5% 1/20W MF 201				DPSNK0_HPD	DP_TBTSNK0_HPD AB5
				DPSNK1_3_P	DP_TBTSNK1_ML_P<3> E6
				DPSNK1_3_N	DP_TBTSNK1_ML_N<3> D5
				DPSNK1_2_P	DP_TBTSNK1_ML_P<2> E8
				DPSNK1_2_N	DP_TBTSNK1_ML_N<2> D7
				DPSNK1_1_P	DP_TBTSNK1_ML_P<1> E10
				DPSNK1_1_N	DP_TBTSNK1_ML_N<1> D9
				DPSNK1_0_P	DP_TBTSNK1_ML_P<0> E12
				DPSNK1_0_N	DP_TBTSNK1_ML_N<0> D11
				DPSNK1_AUX_P	DP_TBTSNK1_AUXCH_P H3
				DPSNK1_AUX_N	DP_TBTSNK1_AUXCH_N H1
R2831 100K 5% 1/20W MF 201				DPSNK1_HPD	DP_TBTSNK1_HPD U4
	TBT_A_R2D_C_P<0>		G24	PA_CIO0_TX_P/DPSRC_0_P	PB_CIO2_TX_P/DPSRC_0_P
	TBT_A_R2D_C_N<0>		E24	PA_CIO0_TX_N/DPSRC_0_N	PB_CIO2_TX_N/DPSRC_0_N
	TBT_A_D2R_P<0>		G22	PA_CIO0_RX_P	PB_CIO2_RX_P
	TBT_A_D2R_N<0>		E22	PA_CIO0_RX_N	PB_CIO2_RX_N
	TBT_A_CONFIG1_BUF		P1	PA_CONFIG1/CIO_0_LSEO	PB_CONFIG1/CIO_2_LSEO
	TBT_A_CONFIG2_RC		K5	PA_CONFIG2/CIO_0_LSOE	PB_CONFIG2/CIO_2_LSOE
	TBT_A_R2D_C_P<1>		L24	PA_CIO1_TX_P/DPSRC_2_P	PB_CIO3_TX_P/DPSRC_2_P
	TBT_A_R2D_C_N<1>		J24	PA_CIO1_TX_N/DPSRC_2_N	PB_CIO3_TX_N/DPSRC_2_N
	TBT_A_D2R_P<1>		L22	PA_CIO1_RX_P	PB_CIO3_RX_P
	TBT_A_D2R_N<1>		J22	PA_CIO1_RX_N	PB_CIO3_RX_N
	TBT_A_LSTX		N8	PA_LSTX/CIO_1_LSEO	PB_LSTX/CIO_3_LSEO
	TBT_A_LSRX		J6	PA_LSRX/CIO_1_LSOE	PB_LSRX/CIO_3_LSOE
	DP_TBTPA_ML_C_P<1>		A16	PA_DPSRC_1_P	PB_DPSRC_1_P
	DP_TBTPA_ML_C_N<1>		B17	PA_DPSRC_1_N	PB_DPSRC_1_N
	DP_TBTPA_ML_C_P<3>		A18	PA_DPSRC_3_P	PB_DPSRC_3_P
	DP_TBTPA_ML_C_N<3>		B19	PA_DPSRC_3_N	PB_DPSRC_3_N
	DP_TBTPA_AUXCH_C_P		L4	PA_AUX_P	PB_AUX_P
	DP_TBTPA_AUXCH_C_N		L2	PA_AUX_N	PB_AUX_N
	DP_TBTPA_HPD		M3	PA_DPSRC_HPD	PB_DPSRC_HPD
	TBT_A_HV_EN		R8	GPIO_0/PA_HV_EN/BYP0	GPIO_1/PB_HV_EN/BYP0
	TBT_A_CIO_SEL		N2	GPIO_10/PA_CIO_SEL/BYP1	GPIO_11/PB_CIO_SEL/BYP1
	TBT_A_DP_PWRDN		P3	GPIO_12/PA_DP_PWRDN/BYP2	GPIO_13/PB_DP_PWRDN/BYP2

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

R2890 3.3K 5% 1/20W MF 201 — R2891 3.3K 5% 1/20W MF 201 — C2890 1UF 10% 6.3V CERM 402 — R2892 3.3K 5% 1/20W MF 201 — R2893 3.3K 5% 1/20W MF 201

BYPASS=U2890 2mm

CRITICAL
OMIT_TABLE

U2890 4MBIT W25X40CLXIG USON

TBT_SPI_MOSI	DI/IO0	
TBT_SPI_CLK	CLK	
TBT_SPI_CS_L	CS*	
TBTROM_WP_L	WP*	
TBTROM_HOLD_L	HOLD*	
	DO/IO1	TBT_SPI_MISO
	VCC	PP3V3_TBTLC
	GND THRM_PAD	

OMIT
R2815 NOSTUFF NONE NONE NONE 0201

DEBUG For monitoring current/voltage
TBT_MONOBSP — MONOBSP
TBT_MONOBSN — MONOBSN

DEBUG For monitoring clock
TP_TBT_THERM_DP — THERMDA
Use AA8 GND ball for THERM DN

TBT_SPI_MOSI	EE_DI AA2
TBT_SPI_MISO	EE_DO Y3
TBT_SPI_CS_L	EE_CS_N T5
TBT_SPI_CLK	EE_CLK U8

R2829 10K 5% 1/20W MF 201

XDP_JTAG_ISP_TDI	TDI W2
JTAG_TBT_TMS	TMS AB1
XDP_JTAG_ISP_TCK	TCK AA6
JTAG_TBT_TDO	TDO U6
TBT_TEST_EN	TEST_EN R6
TBT_TEST_PWR_GOOD	TEST_PWR_GOOD W8

R2825 100 5% 1/20W MF 201

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C2820 0.1UF	DP_TBTSNK0_ML_P<0>	
DP_TBTSNK0_ML_C_N<0>	C2821 0.1UF	DP_TBTSNK0_ML_N<0>	
DP_TBTSNK0_ML_C_P<1>	C2822 0.1UF	DP_TBTSNK0_ML_P<1>	
DP_TBTSNK0_ML_C_N<1>	C2823 0.1UF	DP_TBTSNK0_ML_N<1>	
DP_TBTSNK0_ML_C_P<2>	C2824 0.1UF	DP_TBTSNK0_ML_P<2>	
DP_TBTSNK0_ML_C_N<2>	C2825 0.1UF	DP_TBTSNK0_ML_N<2>	
DP_TBTSNK0_ML_C_P<3>	C2826 0.1UF	DP_TBTSNK0_ML_P<3>	
DP_TBTSNK0_ML_C_N<3>	C2827 0.1UF	DP_TBTSNK0_ML_N<3>	
DP_TBTSNK0_AUXCH_C_P	C2828 0.1UF	DP_TBTSNK0_AUXCH_P	
DP_TBTSNK0_AUXCH_C_N	C2829 0.1UF	DP_TBTSNK0_AUXCH_N	

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0>	C2830 0.1UF	DP_TBTSNK1_ML_P<0>	
DP_TBTSNK1_ML_C_N<0>	C2831 0.1UF	DP_TBTSNK1_ML_N<0>	
DP_TBTSNK1_ML_C_P<1>	C2832 0.1UF	DP_TBTSNK1_ML_P<1>	
DP_TBTSNK1_ML_C_N<1>	C2833 0.1UF	DP_TBTSNK1_ML_N<1>	
DP_TBTSNK1_ML_C_P<2>	C2834 0.1UF	DP_TBTSNK1_ML_P<2>	
DP_TBTSNK1_ML_C_N<2>	C2835 0.1UF	DP_TBTSNK1_ML_N<2>	
DP_TBTSNK1_ML_C_P<3>	C2836 0.1UF	DP_TBTSNK1_ML_P<3>	
DP_TBTSNK1_ML_C_N<3>	C2837 0.1UF	DP_TBTSNK1_ML_N<3>	
DP_TBTSNK1_AUXCH_C_P	C2838 0.1UF	DP_TBTSNK1_AUXCH_P	
DP_TBTSNK1_AUXCH_C_N	C2839 0.1UF	DP_TBTSNK1_AUXCH_N	

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

SYNC_MASTER=T29_RR SYNC_DATE=01/19/2013

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U2940

Part	TPS22920
Type	Load Switch
R(on) @ 1 05V	8 mOhm Typ 11 5 mOhm Max

Max Current = 4A (85C)

1.05V TBT "CIO" Switch

Internal switch not functional on RR

U2940 TPS22920 CSP — VOUT, VIN, CRITICAL, ON, GND

PP1V05_TBT 26 62 — TBT_EN_CIO_PWR — C2940 1 0UF 20% 6 3V X5R 0201 1

PP3V3_TBTLC 17 18 25 26 60 62 — R2945 100K 5% 1/20W MF 201

Q2945 DMN5L06VK-7 SOT563 VER 3

PP3V3_S0 — VER 5 — Q2945 DMN5L06VK-7 SOT563

TBT_PWR_REQ_L (OUT 13) — Pull up (S0) on PCH page — TBT_EN_CIO_PWR_L (IN 25)

U2800 FALCON-RIDGE-FR2C FCBGA SYM 2 OF 2

CRITICAL OMIT_TABLE

VCC1P0_CIO

PP1V05_TBTRDV — MIN LINE WIDTH 0 38 MM, MIN NECK WIDTH 0 20 MM, VOLTAGE 1 05V — 700 mA EDP

C2900–C2906 1 0UF 20% 6 3V X5R 0201 1

G10 G12 G14 G16 G18 H19 H9 J18 K15 K17 K19 K7 L16 M19 P19 T19 U18 V15 V17 W12 W14

VCC1P0_RDV_DECAP

J10 J12 K11 L10 M11 N10 N14 P11 P15 R10 R14 T11 T15 U10 U14 V11

C2930–C2932 1 0UF 20% 6 3V X5R 0201 1 — 62 68 PP1V05_TBTCIO — MIN LINE WIDTH 0 4 MM, MIN NECK WIDTH 0 2 MM, VOLTAGE 1 05V — 1200 mA EDP

VCC

VCC3P3

D1 E2 H11 N4 V5 W4

SVR input to RR 1100 mA EDP

POC input to RR 150 mA EDP

Isolated to reduce noise from SVR

VCC3P3_LC

Y5 — PP3V3_TBTLC — MIN LINE WIDTH 0 4 MM, MIN NECK WIDTH 0 2 MM, VOLTAGE 3 3V — 17 18 25 26 60 62 — 100 mA EDP

C2970 1 0UF 20% 6 3V X5R 0201 1

VCC3P3_RDV_DECAP

H13 H15 H17 H7 L18 N18 R18 W10

PP3V3_TBTRDV — MIN LINE WIDTH 0 38 MM, MIN NECK WIDTH 0 20 MM, VOLTAGE 3 3V — 25 mA EDP

C2980 C2981 1 0UF 20% 6 3V X5R 0201 1

G20 G6 G8 H21 H23 J14 J16 J20 K13 K21 K23 L12 L20 M13 M21 M23 M9 N12 N16 N20 P13 P21 P23 P9 R12 R16 R20 T13 T17 T21 T23 T9 U12 U16 V13 V21 V23 V9 Y11 Y13 Y15 Y17 Y19 Y21 Y23 Y9

GND

C2950–C2953 10UF 20% 6 3V CERM X5R 0402 1 — PLACE NEAR C2953 1 1mm — XW2960

PP3V3_S4 — 25 26 27 29 34 36 37 56 60 62 — 3 1 W (Dual Port) 2 4 W (Single Port) EDP 1 25 A

C2960 C2961 1 0UF 20% 6 3V X5R 0201 1 — PP3V3_S4_TBT_F — MIN LINE WIDTH 0 38 MM, MIN NECK WIDTH 0 20 MM, VOLTAGE 3 3V

62 26 PP1V05_TBT — MIN LINE WIDTH 0 50 MM, MIN NECK WIDTH 0 20 MM, VOLTAGE 1 05V

C2910 C2911 1 0UF 20% 6 3V X5R 0201 1

J8 K9 L14 M15 M17 P17 V19

SVR_VCC1P0

1900 mA EDP

C2923 C2922 C2921 C2920 10UF 20% 6 3V CERM X5R 0402 1

CRITICAL L2920 0.68UH-20%-4.2A-0.032OHM PIMB041B-SM

P1V05TBT_SW — MIN LINE WIDTH 0 50 MM, MIN NECK WIDTH 0 20 MM, DIDT TRUE, SWITCH NODE TRUE

A4 A6 B3

SVR_IND

NCX B5

SVR_AMON

CRITICAL D2920 NSR1020MW2T1G

A2 A24 AA14 AA20 AA22 AA8 AB11 AB17 AC10 AC12 AC14 AC16 AC18 AC20 AC22 AC4 AC6 AC8 B1 B7 C10 C12 C14 C16 C18 C2 C20 C22 C24 C4 C6 C8 D21 D23 E4 F11 F13 F15 F17 F19 F21 F23 F5 F7 F9

VSS — **VSS**

TBT "POC" Power-up Reset

62 60 56 37 36 34 29 27 26 25 PP3V3_S4 — 36 35 27 17 SMC_DELAYED_PWRGD (IN) — 34 30 26 18 17 15 13 12 11 8 57 54 43 42 41 40 39 33 37 36 PP3V3_S0

Q2995 DMN32D2LFB4 SOT563 SYM VER 3

R2995 100K 5% 1/20W MF 201 — R2990 100K 5% 1/20W MF 201 — R2992 100K 5% 1/20W MF 201

CRITICAL U2990 TPS3895ADRY USON — VCC — ENABLE, SENSE, GND, SENSE_OUT, CT

C2990 0 1UF 10% 25V X5R 402 — Push pull output

15 TBT_POC_RESET_L (IN) — TBTPOCRST_MR_L — TBTPOCRST_SENSE — TBTPOCRST_CT — TBT_PWR_ON_POC_RST_L (OUT 25)

C2995 330PF 10% 10V X7R-CERM 0201 — R2991 24 9K 1% 1/20W MF 201 — C2991 0 001UF 10% 50V X7R-CERM 0402

Vth = 2 508V nominal — Delay = 4 04ms nominal

EDP current / power consumption figures copied from R68 schematic (Rev 2 dated October 28 2012 not available on IBL)

SYNC MASTER=T29 RR — SYNC DATE=12/17/2012

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Page Notes

Power aliases required by this page
- =PPVIN SW TBTBST (8 13V Boost Input)
- =PP15V TBT REG (15V Boost Output)

Signal aliases required by this page
(NONE)

BOM options provided by this page
(NONE)

TBT 15V Boost Regulator

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

60 54 48 47 40 39 62 PPBUS_G3H
8-13V Input
Changes required
for 2S.

CRITICAL
Q3080
SI8409DB
BGA

62 60 PPVIN_S4SW_TBTBST_FET
MIN LINE WIDTH=0 5 mm
MIN NECK WIDTH=0 25 mm
Voltage not specified here
add property on another page

R3080 470K 5% 1/20W MF 201
C3080 0.1UF 10% 25V X5R 402
TBTBST_PWREN_DIV_L
R3081 150K 5% 1/20W MF 201
TBTBST_PWREN_L

Q3005
DMN32D2LFB4
SYM VER 2
28 25 IN TBT_A_HV_EN

C3090 10UF 20% 25V X5R CERM 0603
C3091 10UF 20% 25V X5R CERM 0603

R3091 200K 1% 1/20W MF 201
<R1>
TBTBST_EN_UVLO

CRITICAL
L3095
6.8UH-4.0A
PIMB062D SM

CRITICAL
D3095
POWERDI 123
DFLS230L
PP15V_TBT
28 60 62
Vout = 15.1V
Max Current = 1.0A
Freq = 300KHz

TBTBST_BOOST
MIN LINE WIDTH=0 5 mm
MIN NECK WIDTH=0 25 mm
SWITCH NODE=TRUE
DIDT=TRUE

R3089 0 5% 1/20W MF 0201
TBTBST_SNS1
MIN LINE WIDTH=0 2 mm
MIN NECK WIDTH=0 2 mm

TBTBST_SNS2
MIN LINE WIDTH=0 2 mm
MIN NECK WIDTH=0 2 mm

XW3095 SM
PLACE NEAR=C3095 1 2 mm

TBTBST_VSNS
MIN LINE WIDTH=0 2 mm
MIN NECK WIDTH=0 2 mm

CRITICAL
U3090
LT3957
QFN

VIN	27	
SW	8 9 20 21 28	
EN/UVLO	25	TBTBST_EN_UVLO
INTVCC	28	TBTBST_INTVCC
VC	30	TBTBST_VC
RT	33	TBTBST_RT
SS	32	TBTBST_SS
SYNC	34	
SNS1	6	
SNS2	3	
NC	1 2 16 35 36	NC
FBX	31	TBTBST_FBX
SGND	4 23 24 37	
GND	12 13 14 15 16 17	

SGND shorted to
GND inside package
no XW necessary

R3090 49.9K 1% 1/10W MF LF 402
R3095 133K 1% 1/10W MF LF 402
<Ra>
R3096 15.8K 1% 1/10W MF LF 402
<Rb>
Vout = 1.6V * (1 + Ra / Rb)

C3088 22PF 5% 50V CERM 0402
NO STUFF
C3089 100PF 5% 50V CERM 402

C3095 10UF 20% 25V X5R CERM 0603
C3096 10UF 20% 25V X5R CERM 0603
C3097 10UF 20% 25V X5R CERM 0603
C3098 10UF 20% 25V X5R CERM 0603
C3084 10UF 20% 25V X5R CERM 0603
C3085 10UF 20% 25V X5R CERM 0603
C3309A 10UF 20% 25V X7R CERM 0603
C3309B 10UF 20% 25V X5R CERM 0603
C3099 0.001UF 10% 50V X7R CERM 0402

C3081 2.2UF 20% 10V X5R CERM 402
C3092 2.2UF 20% 10V X5R CERM 402
C3087 47PF 5% 25V NP0 C0G CERM 0201
C3093 3300PF 10% 10V X7R CERM 0201
R3093 10K 1% 1/20W MF 201
R3094 41.2K 1% 1/20W MF 201
C3094 0.33UF 10% 6.3V CERM X5R 402
R3092 73.2K 1% 1/20W MF 201
<R2>
C3082 2.2UF 20% 10V X5R CERM 402

TBTBST_VC_RC
TBTBST_VC
MIN LINE WIDTH=0 2 mm
MIN NECK WIDTH=0 2 mm
TBTBST_SS
GND_TBTBST_SGND
MIN LINE WIDTH=0 5 mm
MIN NECK WIDTH=0 25 mm
VOLTAGE=0V

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

Q3088
DMN5L06VK-7
SOT563
VER 3
Max Vgs 10V
R3088 330K 5% 1/20W MF 201
TBTBST_SHDN_DIV
R3087 330K 5% 1/20W MF 201

Q3088
DMN5L06VK-7
SOT563
VER 3
SMC_DELAYED_PWRGD
IN 17 26 35 36

BATLOW# Isolation

Q3000
DMN32D2LFB4
SYM VER 3
35 13 IN PM_BATLOW_L
PP3V3_S4 25 26 29 34 36 37 56 60 62
Pull up on RR page
TBT_BATLOW_L OUT 25 27
TBT_BATLOW_L 25 27
MAKE_BASE_TRUE

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012
PAGE TITLE: TBT Power Support
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices

PP3V3_S5

CRITICAL
C3287 100UF 20% 6.3V POLY TANT CASE B2 SM
C3280 22UF 20% 6.3V X5R CERM 1 603
C3281 0.1UF 10% 16V X5R CERM 0201

PP15V_TBT
15 75V Max

C3215 4.7UF 10% 25V X5R CERM 0603
C3210 0.1UF 10% 25V X5R 402

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S 9 12 6V 7 5 11 7W)

CRITICAL
U3210
CD3211A1RGP
QFN

V3P3
VHV
ENHVU
EN
HV_EN
S0
V3P3OUT
OUT
FAULTZ
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD

S4_PWR_EN
TBT_A_HV_EN
PM_SLP_S3_BUF_L

C3285 0.1UF 10% 16V X5R CERM 0201
C3286 10UF 20% 6.3V CERM X5R 0402

PP3V3_S4_TBTAPWR
MIN LINE WIDTH = 0.38 MM
MIN NECK WIDTH = 0.20 MM
VOLTAGE = 3.3V

PP3V3RHV_S4_TBTAPWR
MIN LINE WIDTH = 0.38 MM
MIN NECK WIDTH = 0.20 MM
VOLTAGE = 15V

C3211 0.1UF 10% 25V X5R 402

TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3

TBTHV_P15V
R3210 22.6K 1% 1/20W MF 201
R3211 22.6K 1% 1/20W MF 201
R3212 36.5K 1% 1/20W MF 201 <RV3P3>

12V See below

TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R

R3213 22.6K 1% 1/20W MF 201 <RHVS3>
R3214 22.6K 1% 1/20W MF 201 <RHVS0>

Single fault protection
requires two R's per HV
ISET Sx with CD3210
Single R on ISET V3P3 OK

ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES MTL FILM 1/20W 17.8K 1 0201 SMD LF	R3210 R3213		TBTHV_P12V
118S0145	2	RES MTL FILM 1/20W 17.8K 1 0201 SMD LF	R3211 R3214		TBTHV_P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector A

PP3V3_S4_TBTAPWR

C3220 0.1UF 10% 16V X5R CERM 0201

SIGNAL MODEL TBT MUX
VDD
CRITICAL
U3220
CBTL05024
HVQFN24 COMBO

TB-		TB_ENA	TBT_A_CIO_SEL
TB+		AUXIO_EN	TBTDP_AUXIO_EN
		DP_PD	TBT_A_DP_PWRDN
AUX-		(IPU) AUXIO-	TBT_A_D2R1_AUXDDC_N
AUX+		(IPD) AUXIO+	TBT_A_D2R1_AUXDDC_P
DDC_DAT			TBT RX 1
DDC_CLK			
CA_DETOUT		CA_DET	TBT_A_CONFIG1_RC
DP+			
DP-			
		DPML0+	DP_A_LSX_ML_P<1>
		DPML0-	DP_A_LSX_ML_N<1>
LSTX	(IPU)		TBT LSX A R2P/P2R (P/N)
LSRX	(IPO)		
HPDOUT		HPD	TBT_A_HPD
GND_THMPAD			

GND VOID TRUE (Both C's)

TBT_A_D2R_N<1>	C3277 0.47UF		TBT_A_D2R_C_N<1>
TBT_A_D2R_P<1>	C3276 0.47UF		TBT_A_D2R_C_P<1>
DP_TBTPA_AUXCH_C_N	C3230 0.1UF		DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_C_P	C3231 0.1UF		DP_TBTPA_AUXCH_P
			DP_TBTSNK0_DDC_DATA
			DP_TBTSNK0_DDC_CLK
			TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1>	C3232 0.22UF		DP_TBTPA_ML_P<1>
DP_TBTPA_ML_C_N<1>	C3233 0.22UF		DP_TBTPA_ML_N<1>
			TBT_A_LSTX
			TBT_A_LSRX
			DP_TBTPA_HPD

CRITICAL
L3200
FERR 120 OHM 3A 0603

PP3V3RHV_S4_TBTAPWR_F
MIN LINE WIDTH = 0.38 MM
MIN NECK WIDTH = 0.20 MM
VOLTAGE = 15V

C3200 0.01UF 10% 50V X7R CERM 0402

TBTACONN_20_RC
MIN LINE WIDTH = 0.38 MM
MIN NECK WIDTH = 0.20 MM
VOLTAGE = 18V

R3201 12 5% 1/20W MF 201

C3201 0.01UF 10% 50V X7R CERM 0402

TBTACONN_1_C
MIN LINE WIDTH = 0.38 MM
MIN NECK WIDTH = 0.20 MM
VOLTAGE = 18.9V

(0 18 9V)

C3205 0.01UF 10% 25V X5R CERM 0201

GND VOID TRUE (Both C's)

TBT_A_D2R_P<0>	C3274 0.47UF		TBT_A_D2R_C_P<0>
TBT_A_D2R_N<0>	C3275 0.47UF		TBT_A_D2R_C_N<0>
			TBT TX 0
			TBT RX 0
DP_TBTPA_ML_C_P<3>	C3278 0.22UF		DP_TBTPA_ML_P<3>
DP_TBTPA_ML_C_N<3>	C3279 0.22UF		DP_TBTPA_ML_N<3>
			TBT Unused
			TBT_A_D2R1_AUXDDC_P
			TBT_A_D2R1_AUXDDC_N
			TBT RX 1

R3294 1K 5% 1/20W MF 201 NO XNET CONNECTION TRUE
R3295 1K 5% 1/20W MF 201 NO XNET CONNECTION TRUE

R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201

TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC

C3202 0.01UF 10% 16V X5R CERM 0201

DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1 1a)

Sink HPD range
High 2.0 5.0V
Low 0 0.8V

R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R CERM 0201
C3295 330PF 10% 16V X7R CERM 0201
R3241 100K 5% 1/20W MF 201

J3200
MDP-J11
F-RT-TH
CRITICAL
514-0818

2	HOT_PLUG_DETECT	GND	1
4	CONFIG1	ML_LANE0P	3
6	CONFIG2	ML_LANE0N	5
13	GND	GND	7
10	ML_LANE3P	ML_LANE1P	9
12	ML_LANE3N	ML_LANE1N	11
14	GND	GND	8
16	AUX_CHP	ML_LANE2P	15
18	AUX_CHN	ML_LANE2N	17
20	DP_PWR	RETURN	19

SHIELD PINS 28 27 26 25 24 23 22 21

TBTACONN_7_C
MIN LINE WIDTH = 0.38 MM
MIN NECK WIDTH = 0.20 MM
VOLTAGE = 18.9V

(0 18 9V)

C3206 0.01UF 10% 25V X5R CERM 0201

DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT LSX R2P/P2R (P/N)

C3270 0.22UF 20% 6.3V X5R 0201
C3271 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>

R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201

C3272 0.22UF 20% 6.3V X5R 0201
C3273 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>

R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201

470k R's for ESD protection
on AC coupled signals

SYNC MASTER=T29_RR SYNC DATE=10/26/2012

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Apple Inc.

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3.3V WLAN Switch

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

Sense resistor on sensor page

PP3V3_WLAN
MIN LINE WIDTH=0.5 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=3.3V
35 36 37 39 62

PP3V3_WLAN_R
MIN LINE WIDTH=0.5 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=3.3V
39

Max Current = 2A (85C)

U3550
TPS22924
CSP
A1 VOUT
B1
A2 VIN
B2
CRITICAL
C2 ON
GND
C1

PP3V3_S5
8 11 13 15 16 17 18 28 29 40 52 55 56 57 58 60 62 72

SMC_WIFI_PWR_EN <IN> 29 35 37

C3550
1.0UF
20%
6.3V
X5R
0201 1

514S0335
CRITICAL
J3501
SSD-K99
F RT SH1

C3521
0.1UF
10%
6.3V
CERM X5R
0201
BYPASS=J3501 5mm

AIRPORT

67 62 PCIE_AP_R2D_N	C3531 0.1UF 10% XSR CERM 16V 0201	PCIE_AP_R2D_C_N	<IN> 14 67
67 62 PCIE_AP_R2D_P	C3530 0.1UF 10% XSR CERM 16V 0201	PCIE_AP_R2D_C_P	<IN> 14 67
		PCIE_CLK100M_AP_N	<IN> 12 62 67
		PCIE_CLK100M_AP_P	<IN> 12 62 67
		PCIE_AP_D2R_P	<OUT> 14 62 67
		PCIE_AP_D2R_N	<OUT> 14 62 67
		WIFI_EVENT_L	<OUT> 35 36 62

PP3V3_S4 25 26 27 29 34 36 37 56 60 62

C3532
0.1UF
10%
6.3V
CERM X5R
0201
BYPASS=J3501 1 5mm

Supervisor & CLKREQ# Isolation

Delay = 130 ms +/- 20%

APCLKRQ:ISOL
R3553
100K
5%
1/20W
MF
201

R3554
232K
1%
1/20W
MF
201

P3V3WLAN_VMON

U3540
SLG4AP041V
TDFN
CRITICAL
VDD
SENSE
VREF
*DLY
RESET*
MR*
EN
OUT (OD)
IN
THRM PAD
GND

PP3V3_S5
8 11 13 15 16 17 18 28 29 40 52 55 56 57 58 60 62 72

C3540
0.1UF
10%
6.3V
CERM X5R
0201

R3558
0
5%
1/20W
MF
0201

62 AP_RESET_CONN_L
AP_RESET_CONN_R_L
AP_RESET_L <IN> 15

SMC_WIFI_PWR_EN <IN> 29 35 37
AP_CLKREQ_R_L
62 AP_CLKREQ_Q_L

R3555
100K
1%
1/20W
MF
201

APCLKRQ:ISOL
R3556
0
5%
1/20W
MF
0201

APCLKRQ:BIDIR
R3557
0
5%
1/20W
MF
0201
AP_CLKREQ_L <BI> 12

NOSTUFF
R3559
0
5%
1/20W
MF
0201

PCIe Wake Muxing

58 57 56 18 15 14 PP3V3_S5
17 16 15 73 62 60

R3561
100K
5%
1/20W
MF
201

C3560
0.1UF
10%
6.3V
CERM X5R
0201

VCC
CRITICAL
U3560
NC7SB3157P6XG
SC70
VER-3
GND

SEL	OUTPUT
L	PCIE_WAKE_L (B0)
H	AP_S0IX_WAKE_L (B1)

S AP_S0IX_WAKE_SEL <IN> 15
B0 PCIE_WAKE_L <OUT> 13 31 62
B1 AP_S0IX_WAKE_L <OUT> 15
A AP_PCIE_WAKE_L

NOSTUFF
R3560
0
5%
1/20W
MF
0201

36 34 29 27 26 25 22 60 59 57 PP3V3_S4

BLUETOOTH

C3510
0.1UF
10%
6.3V
CERM X5R
0201

U3510
USB3740
DFN
CRITICAL
VDD
DP
DM
DP_2
DM_2
DP_1
DM_1
OE*
S
GND
NC

66 62 USB_BT_CONN_P
66 62 USB_BT_CONN_N
USB_BT_P <BI> 14 66
USB_BT_N <BI> 14 66
BT_WAKE
PM_SLP_S4_L <IN> 13 18 34 35 57

SIGNAL_MODEL=BT_MUX

SEL	OUTPUT
L	BT_WAKE (1)
H	USB_BT (2)

NO XNET CONNECTION=TRUE
Q3510
DMN32D2LFB4
DFN1006H4 3
SYM VER 2
D G S

SMC_PME_S4_WAKE_L <OUT> 34 35 37

R3512
15K
1%
1/20W
MF
201

SYNC_MASTER=J43_MLB
SYNC_DATE=10/02/2012

PAGE TITLE
Wireless Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
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OOB Isolation

PP3V3_S0SW_SSD → C3718 0.1UF 10% 10V X5R CERM 0201 (BYPASS=U3710 5 mm)

U3710 74LVC1G08 SOT891 (CRITICAL)
- 1 NC
- 2 ← SMC_OOB1_R2D_L (IN)
- 3 NC
- 4 ← PP3V3_S0
- 5 NC
- 6 ← PP3V3_S0SW_SSD

U3711 74LVC1G08 SOT891 (CRITICAL)
- 1 NC
- 2 ← PP3V3_S0
- 3 NC
- 4 → SMC_OOB1_D2R_L (OUT)
- 5 NC
- 6 ← PP3V3_S0SW_SSD

C3719 0.1UF 10% 10V X5R CERM 0201 (BYPASS=U3711 5 mm)

R3703 100K 1% 1/20W MF 201 (PP3V3_S0)

R3710 100K 5% 1/20W MF 201 (NOSTUFF)

R3700 100K 1% 1/20W MF 201 (NOSTUFF)

SMC_PWRFAIL_WARN_L Signal no connect on X31

Gumstick3 Connector

514S0449 CRITICAL
J3700 SSD-GS3
F RT SM

GND VOID	1	53		GND VOID
	2	52	62	SMC_OOB1_R2D_CONN_L
	3	51	62	SMC_OOB1_D2R_CONN_L
	4			
	5	50		SSD_PCIE_SEL_L (OUT 30 62)
	6	49		TP_SSD_DEVSLP
	7	48		SMC_PWRFAIL_WARN_L (IN 35 62)
	8	47		SSD_PWR_EN (IN 15 30 56 57 62)
	9			
	10	46		
TRUE	11	45	TRUE	PCIE_SSD_D2R_N<3> (OUT 12 62 65)
TRUE	12	44	TRUE	PCIE_SSD_D2R_P<3> (OUT 12 62 65)
	13	43		
TRUE	14	42	TRUE	PCIE_SSD_D2R_N<2> (OUT 12 62 65)
TRUE	15	41	TRUE	PCIE_SSD_D2R_P<2> (OUT 12 62 65)
	16	40		
	17	39		
TRUE	18	38	TRUE	PCIE_SSD_D2R_N<1> (OUT 12 62 65)
TRUE	19	37	TRUE	PCIE_SSD_D2R_P<1> (OUT 12 62 65)
	20	36		
TRUE	21	35	TRUE	PCIE_SSD_D2R_N<0> (OUT 12 62 65)
TRUE	22	34	TRUE	PCIE_SSD_D2R_P<0> (OUT 12 62 65)
	23	33		
	24			
	25	32		
	26	31		PCIE_CLK100M_SSD_N (IN 12 62 65)
	27	30		PCIE_CLK100M_SSD_P (IN 12 62 65)
	28	29		
	54	59		
	55	60		
	56	61		
	57	62		
	58	63		

PCIe polarity inversion and lane reversal are only permitted on the device side, provided the device PHY supports it.

PP3V3_S0 (34 30 26 18 17 15 13 12 11 8 / 57 54 43 42 41 40 39 38 37 36 / 72 63 62 60 59)

SSD_SR_EN_L (62 15 IN) → SSD_RESET_CONN_L (62) → R3701 0 5% 1/20W NOSTUFF → SSD_BOOT_R (65 62) → SSD_BOOT (18 IN)

PCIE_SSD_R2D_C_N<3> (65 12 IN)	C3710 0.1UF	PCIE_SSD_R2D_N<3> (65 62)	PCIE_SSD_D2R_N<3>
PCIE_SSD_R2D_C_P<3> (65 12 IN)	C3711 0.1UF	PCIE_SSD_R2D_P<3> (65 62)	PCIE_SSD_D2R_P<3>
PCIE_SSD_R2D_C_N<2> (65 12 IN)	C3712 0.1UF	PCIE_SSD_R2D_N<2> (65 62)	PCIE_SSD_D2R_N<2>
PCIE_SSD_R2D_C_P<2> (65 12 IN)	C3713 0.1UF	PCIE_SSD_R2D_P<2> (65 62)	PCIE_SSD_D2R_P<2>
PCIE_SSD_R2D_C_N<1> (65 12 IN)	C3714 0.1UF	PCIE_SSD_R2D_N<1> (65 62)	PCIE_SSD_D2R_N<1>
PCIE_SSD_R2D_C_P<1> (65 12 IN)	C3715 0.1UF	PCIE_SSD_R2D_P<1> (65 62)	PCIE_SSD_D2R_P<1>
PCIE_SSD_R2D_C_N<0> (65 12 IN)	C3716 0.1UF	PCIE_SSD_R2D_N<0> (65 62)	PCIE_SSD_D2R_N<0>
PCIE_SSD_R2D_C_P<0> (65 12 IN)	C3717 0.1UF	PCIE_SSD_R2D_P<0> (65 62)	PCIE_SSD_D2R_P<0>

(C3710–C3717: 10% 16V X5R CERM 0201, GND_VOID=TRUE, MF 0201)

SSD_CLKREQ_CONN_L (62)

Per Intel PDG, use PCIe style decoupling, when muxing PCIe & SATA

R3702 0 5% 1/20W MF 0201: SSD_PCIE_SEL_L (62 30) → GND

Supervisor & CLKREQ# Isolation

Delay = ~55ms

PP3V3_S0SW_SSD (30 39 60 62) → R3740 100K 5% 1/20W MF 201 → P3V3SSD_VMON

R3741 232K 1% 1/20W MF 201

PP3V42_G3H (17 33 34 35 36 38 44 46 47 48 / 57 59 60 62 63) → C3740 0.1UF 10% 6.3V CERM X5R 0201

U3740 SLG4AP016V TDFN (CRITICAL)
- VDD
- 2 SENSE 0.7V → P3V3SSD_VMON
- DLY
- 4 RESET* → SSD_RESET_L (IN 15)
- 3 MR*
- 6 EN ← SSD_PWR_EN (IN 15 30 56 57 62)
- 8 OUT (OD) → SSD_CLKREQ_L (OUT 12)
- 7 IN
- THRM PAD
- 5 GND

R3742 100K 1% 1/20W MF 201

SYNC_MASTER=J43_MLB	SYNC_DATE=02/20/2013
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U3900
BCM15700
FBGA
SYM 3 OF 3
CRITICAL
OMIT_TABLE

MIPI_AGND
DDR_VDDIO
PCIE_GND
PMU_AVSS
SR_PVSSC
SR_PVSSD
VSSC
XTAL_AVSS
DDR_VDDIO_CK
DDR_VREF
PCIE_VDD1P2
PCIE_PVDD1P2
DDR_AVDD1P8
MIPI_AVDD1P8
PLL_VDD1P8
OTP_VDD3P3
SR_VDD_3P3C
SR_VDD_3P3D
SR_VLXC_0
SR_VLXD_0
VDD_1P35A
VDD_3P3A
VDD1P2_O
VDD1P8_O
VDDC
VDD018
XTAL_AVDD1P2

PP1V35_CAM
PP1V35_DDR_CLK
PP0V675_CAM_VREF
PP1V2_CAM_PCIE_VDD_FLT
PP1V2_CAM_PCIE_PVDD_FLT
PP1V8_CAM
PP1V2_CAM_SRVLXC_PHASE
PP1V35_CAM_SRVLXD_PHASE
PP1V2_CAM_XTALPCIEVDD
PP1V2_CAM
GND_CAM_PVSSC
GND_CAM_PVSSD
GND_CAM_PVSSD
PP3V3_S3RS0_CAMERA
(=PP3V3_S3RS0_CAMERA)
L3906 22NH 0402
L3902 1.0UH-1.6A-55MOHM 1008
L3903 220-OHM-1.4A 0603
L3904 220-OHM-1.4A 0603
L3901 1.0UH-1.6A-55MOHM 1008
C3900 0.1UF 10% 6.3V CERM X5R 0201
C3927 0.1UF 10% 6.3V CERM X5R 0201
C3921 1.0UF 20% 6.3V X5R 0201 1
C3922 0.1UF 10% 6.3V CERM X5R 0201
C3923 1.0UF 20% 6.3V X5R 0201 1
C3924 0.1UF 10% 6.3V CERM X5R 0201
C3912 4.7UF 20% 6.3V X5R 402
C3913 4.7UF 20% 6.3V X5R 402
C3930 1.0UF 20% 6.3V X5R 0201 1
C3931 10UF 20% 6.3V CERM X5R 0402 1
C3932 1.0UF 20% 6.3V X5R 0201 1
C3933 10UF 20% 6.3V CERM X5R 0402 1
C3970 0.1UF 10% 6.3V CERM X5R 0201
C3971 1000PF 10% 16V X7R CERM 0201
C3972 0.1UF 10% 6.3V CERM X5R 0201
C3973 1000PF 10% 16V X7R CERM 0201
C3974 0.1UF 10% 6.3V CERM X5R 0201
C3975 0.1UF 10% 6.3V CERM X5R 0201
C3914 4.7UF 20% 6.3V X5R 402
C3915 4.7UF 20% 6.3V X5R 402
C3919 0.1UF 10% 6.3V CERM X5R 0201
C3918 1000PF 10% 16V X7R CERM 0201
C3916 0.1UF 10% 6.3V CERM X5R 0201
C3917 1000PF 10% 16V X7R CERM 0201
C3910 0.1UF 10% 6.3V CERM X5R 0201
C3951 0.1UF 10% 6.3V CERM X5R 0201
C3928 4.7UF 20% 6.3V X5R 402
C3938 1000PF 10% 16V X7R CERM 0201
C3926 4.7UF 20% 6.3V X5R 402
C3942 4.7UF 20% 6.3V X5R 402
C3940 0.1UF 10% 6.3V CERM X5R 0201
C3934 1000PF 10% 16V X7R CERM 0201
C3935 0.1UF 10% 6.3V CERM X5R 0201
C3936 1000PF 10% 16V X7R CERM 0201
C3937 0.1UF 10% 6.3V CERM X5R 0201
C3941 2.2UF 20% 6.3V CERM 402 LF
C3939 1UF 10% 10V X5R 402
C3960 0.1UF 10% 6.3V CERM X5R 0201
XW3900 SM
XW3901 SM
R3930 100K 5% 1/20W MF 201
R3932 100K 5% 1/20W MF 201
R3934 100K 5% 1/20W MF 201
R3931 330K 5% 1/20W MF 201
R3933 330K 5% 1/20W MF 201
R3935 330K 5% 1/20W MF 201
R3920 100K 5% 1/20W MF 201
R3921 100K 5% 1/20W MF 201
R3913 1K 5% 1/20W MF 201
R3914 1K 5% 1/20W MF 201
R3936 100K 5% 1/20W MF 201
R3937 100K 5% 1/20W MF 201
R3991 0 5% 1/20W MF 0201
R3990 100K 5% 1/20W MF 201
R3901 100K 5% 1/20W MF 201
R3915 100K 5% 1/20W MF 201
R3910 100K 5% 1/20W MF 201
R3911 100K 5% 1/20W MF 201
R3904 100K 5% 1/20W MF 201
R3906 100K 5% 1/20W MF 201
R3907 100K 5% 1/20W MF 201
R3912 240 1% 1/20W MF 201
R3975 51K 5% 1/20W MF 201
R3976 51K 5% 1/20W MF 201
C3990 0.1UF 10% 6.3V CERM X5R 0201

NOSTUFF
PLACE_NEAR=U3900.M13:4MM
PLACE_NEAR=U3900.M13:2.54MM
PLACE_NEAR=U3900.M14 2.54MM
PLACE_NEAR=U3900.K13 4MM
BYPASS=U3900 K13 2.54MM
BYPASS=U3900 F6 2.54MM
BYPASS=U3900 F9 2.54MM
BYPASS=U3900 L9 2.54MM
BYPASS=U3900 J1 2.54MM
BYPASS=U3900 L7 2.54MM
BYPASS=U3900 D6 2.54MM
BYPASS=U3900 D7 2.54MM
BYPASS=U3900 7mm
BYPASS=U3900 5mm
BYPASS=U3900 3mm
BYPASS=U3900 F15 2.54MM
BYPASS=U3900 G15 2.54MM
MIN LINE WIDTH=0 6MM
MIN NECK WIDTH=0 2MM
VOLTAGE=1 35V
VOLTAGE=1 2V
VOLTAGE=0 675V
VOLTAGE=0V
MAKE BASE=TRUE
DIDT=TRUE

L3901:1 VSENSE_C
L3902:1 VSENSE_D

MEM_CAM_A<0>
MEM_CAM_A<1>
MEM_CAM_A<2>
MEM_CAM_A<3>
MEM_CAM_A<4>
MEM_CAM_A<5>
MEM_CAM_A<6>
MEM_CAM_A<7>
MEM_CAM_A<8>
MEM_CAM_A<9>
MEM_CAM_A<10>
MEM_CAM_A<11>
MEM_CAM_A<12>
MEM_CAM_A<13>
MEM_CAM_A<14>
DDR_AD00
DDR_AD01
DDR_AD02
DDR_AD03
DDR_AD04
DDR_AD05
DDR_AD06
DDR_AD07
DDR_AD08
DDR_AD09
DDR_AD10
DDR_AD11
DDR_AD12
DDR_AD13
DDR_AD14

MEM_CAM_BA<0>
MEM_CAM_BA<1>
MEM_CAM_BA<2>
DDR_BA0
DDR_BA1
DDR_BA2

MEM_CAM_CLK_P
MEM_CAM_CLK_N
DDR_CK_P0
DDR_CK_N0

MEM_CAM_DM<0>
MEM_CAM_DM<1>
DDR_DM0
DDR_DM1

MEM_CAM_ZQ_S2
MEM_CAM_CKE
MEM_CAM_CS_L
DDR_ZQ
DDR_CKE
DDR_CS*

DDR_DQ00 MEM_CAM_DQ<0>
DDR_DQ01 MEM_CAM_DQ<1>
DDR_DQ02 MEM_CAM_DQ<2>
DDR_DQ03 MEM_CAM_DQ<3>
DDR_DQ04 MEM_CAM_DQ<4>
DDR_DQ05 MEM_CAM_DQ<5>
DDR_DQ06 MEM_CAM_DQ<6>
DDR_DQ07 MEM_CAM_DQ<7>
DDR_DQ08 MEM_CAM_DQ<8>
DDR_DQ09 MEM_CAM_DQ<9>
DDR_DQ10 MEM_CAM_DQ<10>
DDR_DQ11 MEM_CAM_DQ<11>
DDR_DQ12 MEM_CAM_DQ<12>
DDR_DQ13 MEM_CAM_DQ<13>
DDR_DQ14 MEM_CAM_DQ<14>
DDR_DQ15 MEM_CAM_DQ<15>

DDR_DQS_P0 MEM_CAM_DQS_P<0>
DDR_DQS_N0 MEM_CAM_DQS_N<0>
DDR_DQS_P1 MEM_CAM_DQS_P<1>
DDR_DQS_N1 MEM_CAM_DQS_N<1>

DDR_RAS* MEM_CAM_RAS_L
DDR_WE* MEM_CAM_WE_L
DDR_CAS* MEM_CAM_CAS_L
DDR_RESET* MEM_CAM_RESET_L

MIPI_CLK_P
MIPI_CLK_N
MIPI_DATA_P
MIPI_DATA_N
MIPI_CP_CLK
MIPI_CM_CLK
MIPI_DP0
MIPI_DM0
MIPI_DP1
MIPI_DM1

PCIE_CAMERA_R2D_P
PCIE_CAMERA_R2D_N
PCIE_CLK100M_CAMERA_C_P
PCIE_CLK100M_CAMERA_C_N
PCIE_CAMERA_D2R_C_P
PCIE_CAMERA_D2R_C_N
PCIE_RDP0
PCIE_RDN0
PCIE_REFCLKP
PCIE_REFCLKN
PCIE_TDP0
PCIE_TDN0
PCIE_TESTP
PCIE_TESTN

CLK25M_CAM_CLKP
CLK25M_CAM_CLKN
XTAL_P
XTAL_N

I2C_CAM_SMBDBG_CLK
I2C_CAM_SCK
I2C_CAM_SMBDBG_DAT
I2C_CAM_SDA
I2C_CLK_DBG
I2C_CLK_SENSOR
I2C_DATA_DBG
I2C_DATA_SENSOR

TP_CAM_JTAG_TCK
TP_CAM_JTAG_TDI
TP_CAM_JTAG_TDO
TP_CAM_JTAG_TMS
TP_CAM_JTAG_TRST_L
CAM_JTAG_SRST_L
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TRST*
JTAG_SRST*

CAMERA_CLKREQ_L
CAM_PCIE_RESET_L
CAM_PCIE_WAKE_L
PCIE_CLKREQ*
PCIE_RST*
PCIE_WAKE*

CAM_PWR_SEL
CAM_DEBUG_RESET_L
PWR_MODE
RESET*
SENSOR_WAKE*
SHUTDOWN*

CAM_SENSOR_WAKE_L
CAMERA_PWR_EN

PU on PCH page
PD = 1.35V
PU = 25MHz

DEBUG_00 TP_CAM_TEST_MODE0
DEBUG_01 TP_CAM_TEST_MODE1
DEBUG_02 TP_CAM_TEST_MODE2
DEBUG_03 TP_CAM_LV_JTAG_TCK
DEBUG_04 TP_CAM_LV_JTAG_TDI
DEBUG_05 TP_CAM_LV_JTAG_TDO
DEBUG_06 TP_CAM_LV_JTAG_TMS
DEBUG_07 TP_CAM_LV_JTAG_TRSTN
DEBUG_08 NC
DEBUG_09 NC
DEBUG_10 NC
DEBUG_11 NC
DEBUG_12 NC
DEBUG_13 NC
DEBUG_14 NC
DEBUG_15 NC
DEBUG_16 NC

GPIO_00 CAM_RAMCFG0
GPIO_01 CAM_RAMCFG1
GPIO_02 CAM_RAMCFG2
GPIO_03 CAM_GPIO3
GPIO_04 TP_CAM_PLL_BYPASS
GPIO_05 NC
GPIO_06 NC
GPIO_07 NC

UARTCTS CAM_UARTCTS
UARTRTS TP_CAM_UARTRTS
UARTRXD CAM_UARTRXD
UARTTXD TP_CAM_UARTTXD

TEST_OUT CAM_TEST_OUT
TEST_MODE CAM_TEST_MODE
STRAP_XTAL_FREQ CAM_XTAL_FREQ
STRAP_XTAL_SEL CAM_XTAL_SEL

CAM_RAMCFG2
CAM_RAMCFG1
CAM_RAMCFG0
CAM_A1
CAM_TEST_MODE
CAM_TEST_OUT
CAM_UARTCTS
CAM_UARTRXD
CAM_XTAL_FREQ
CAM_XTAL_SEL
CAM_XTAL:YES
CAM_XTAL:NO
A1 SILICON BUG

PCIE_WAKE_L
NOSTUFF
NO STUFF

SYNC_MASTER=J43_MLB1	SYNC_DATE=01/09/2013
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Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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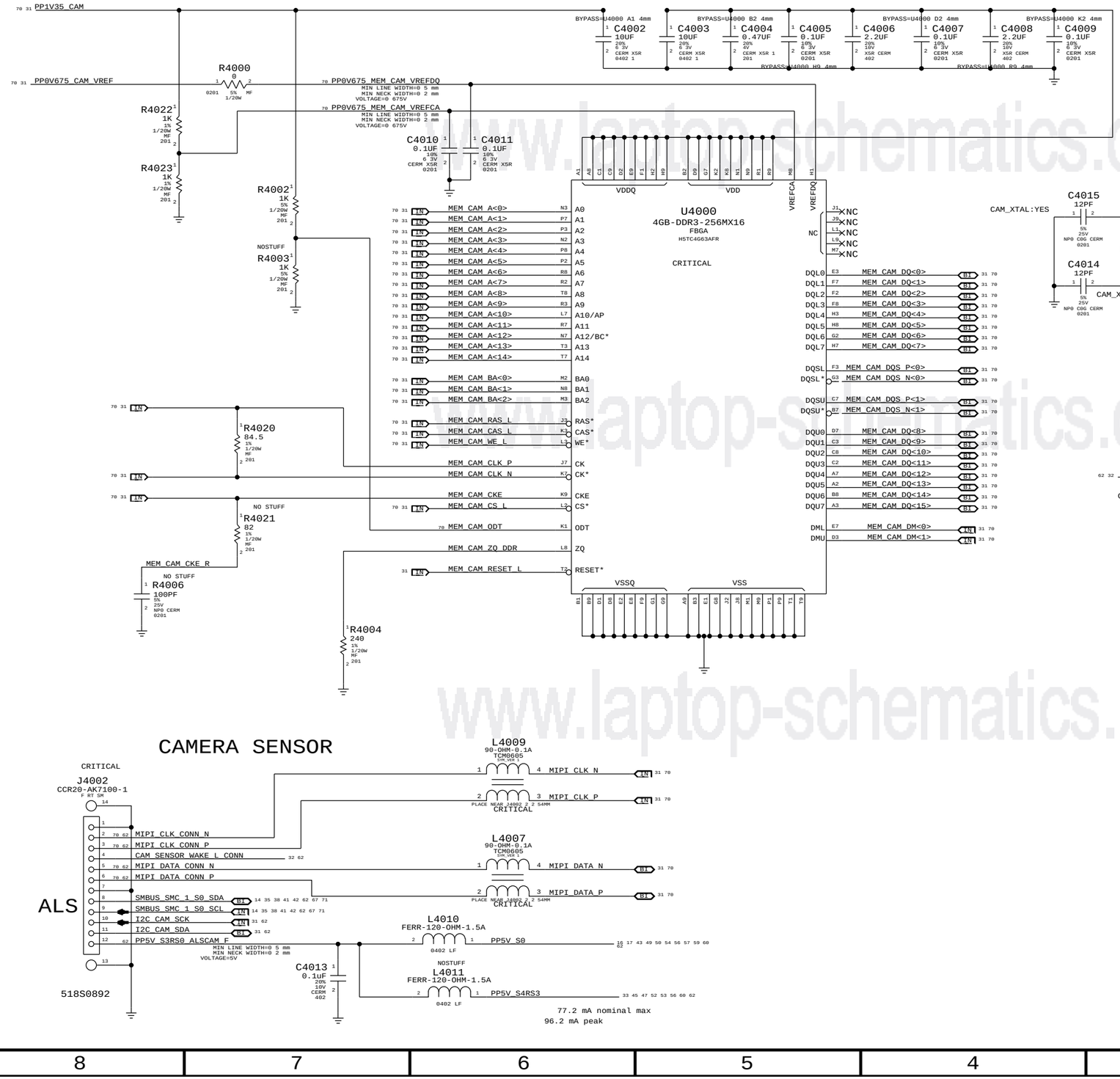

SYNC_MASTER=J43_MLB
SYNC_DATE=09/14/2012

PAGE TITLE
Camera 2 of 2

Apple Inc.

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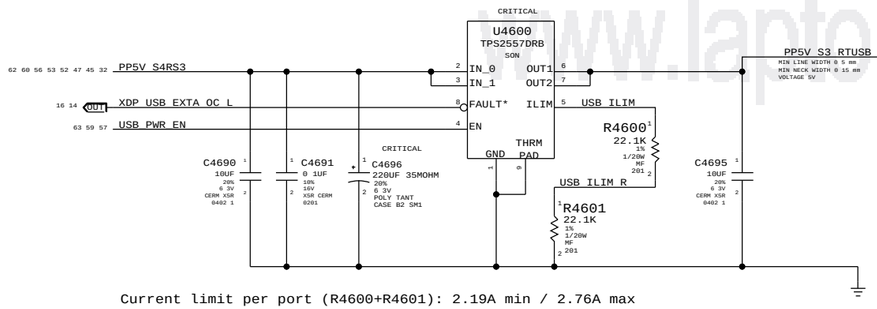
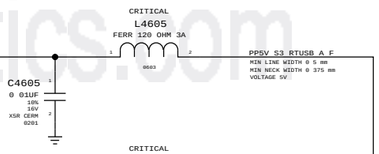
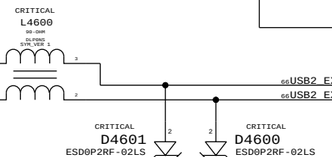
Right USB Port A

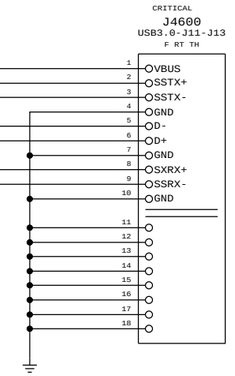
USB Port Power Switch



Current limit per port (R4600+R4601): 2.19A min / 2.76A max

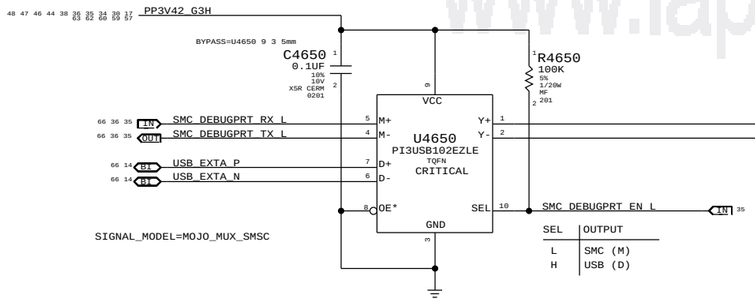


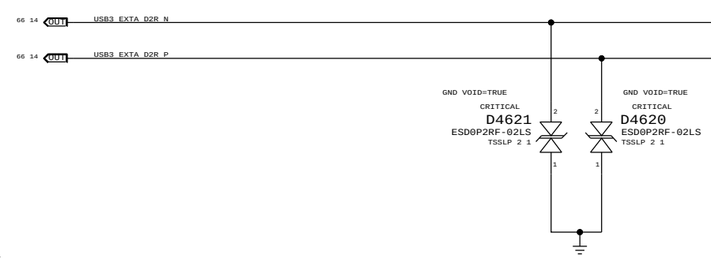


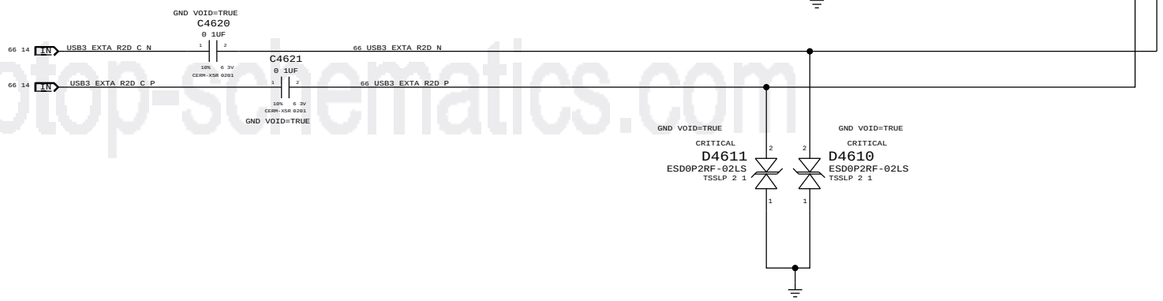


APN: 514-0819

Mojo SMC Debug Mux







SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE: External A USB3 Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

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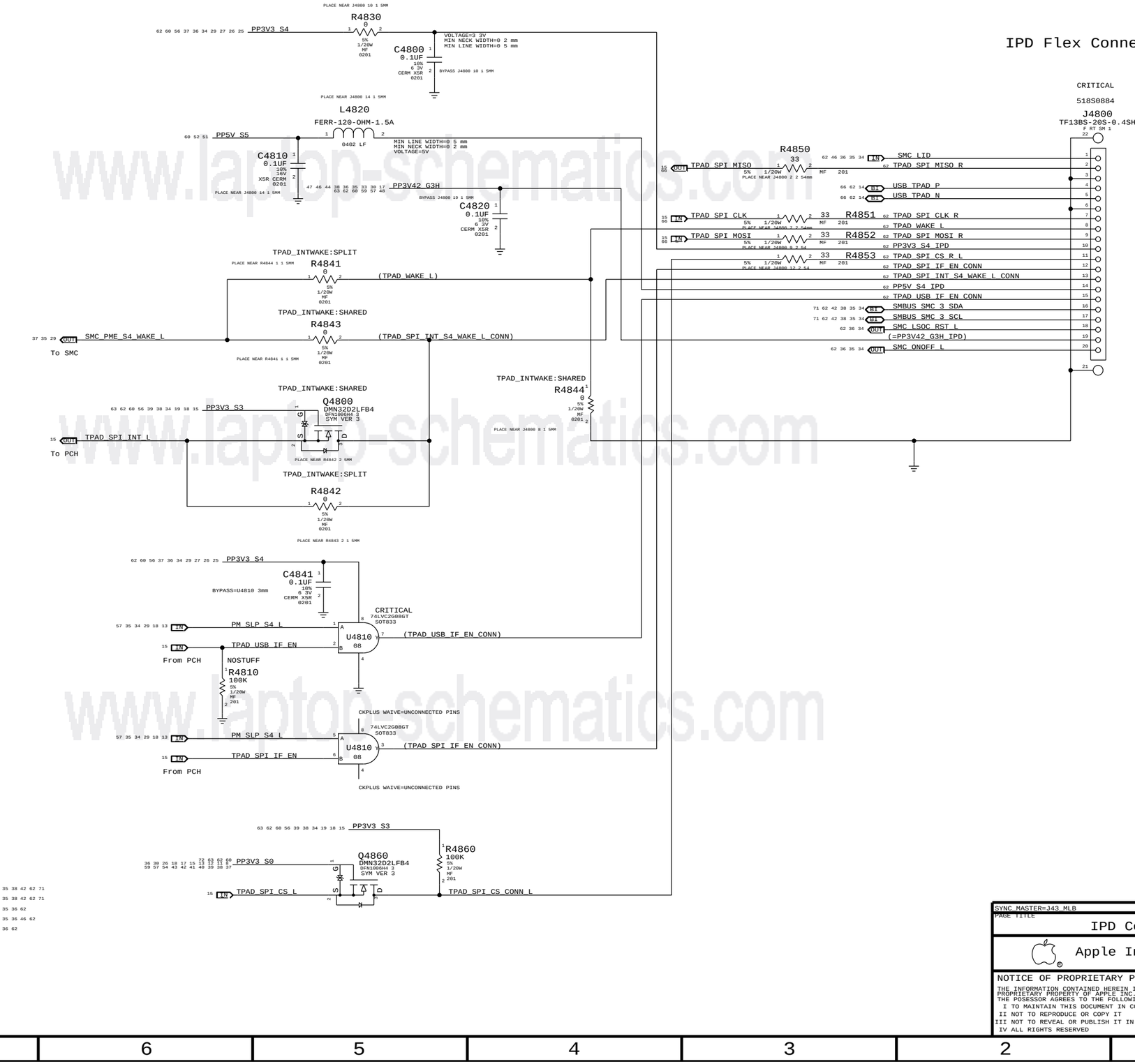
IPD Flex Connector



SYNC_MASTER=J43_MLB SYNC_DATE=01/17/2013

PAGE TITLE: IPD Connector

Apple Inc.

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REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 48 OF 120
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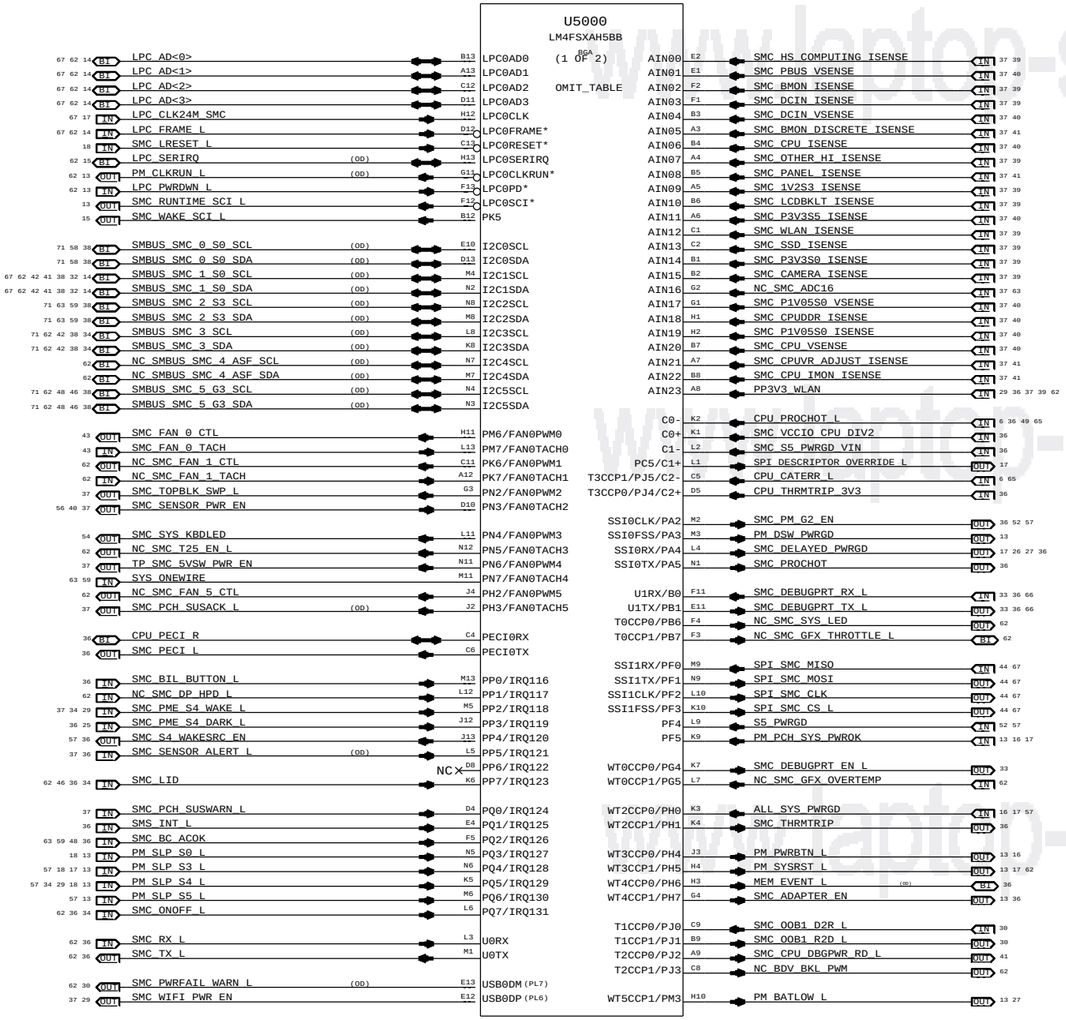

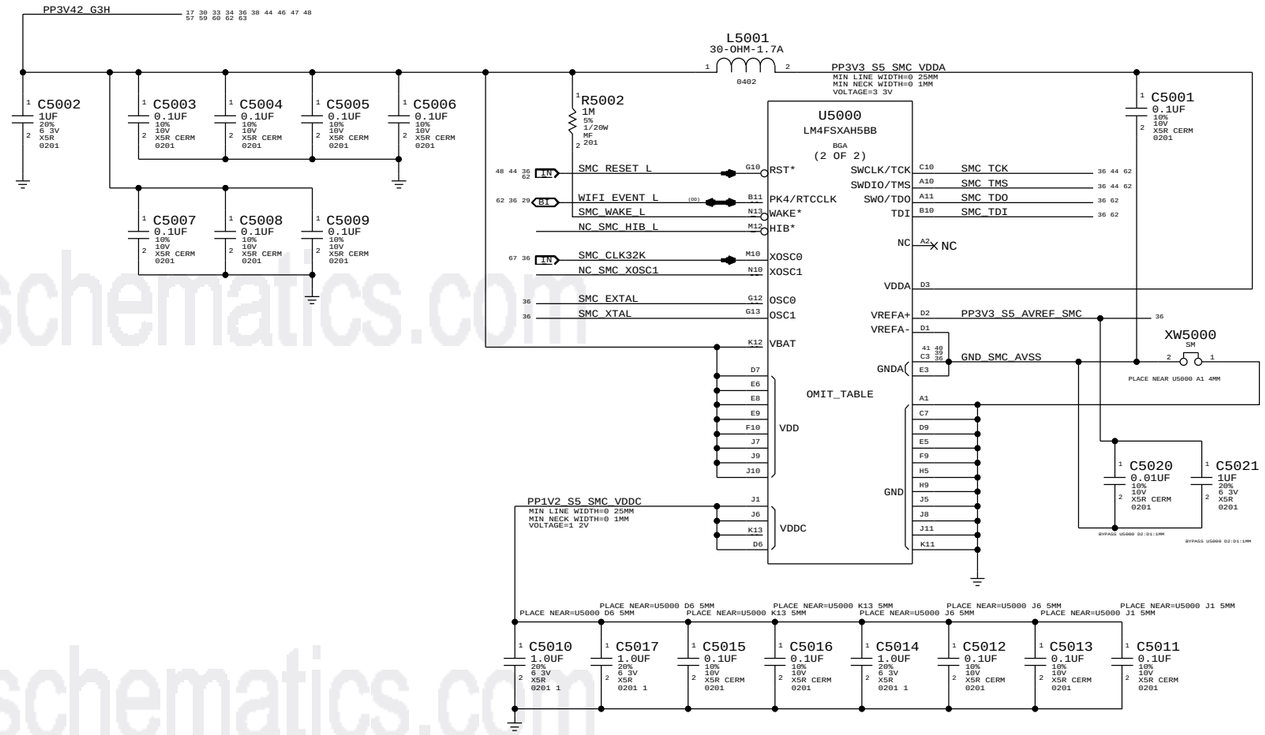

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

SYNC MASTER=WILL J43 SYNC DATE=12/17/2012

PAGE TITLE
SMC

Apple Inc.

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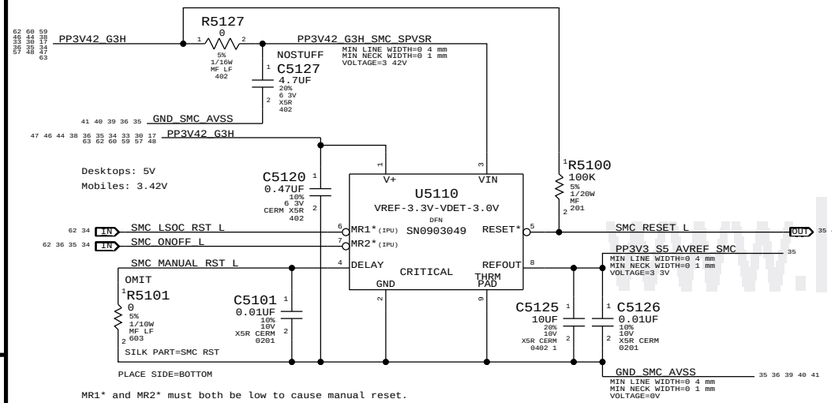
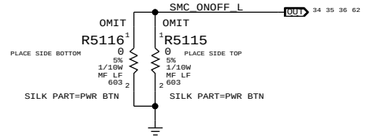
SMC Reset "Button", Supervisor & AVREF Supply



Desktops: 5V
Mobiles: 3.42V

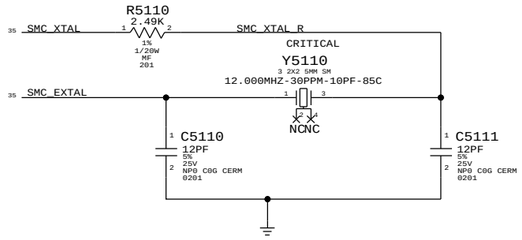
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

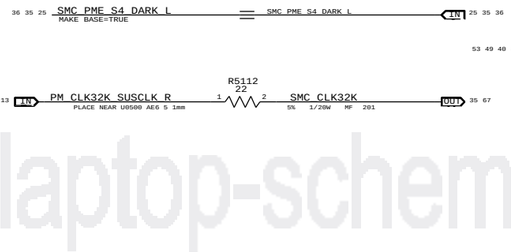
Debug Power "Buttons"

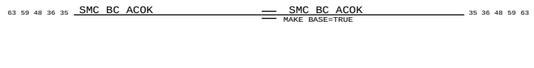


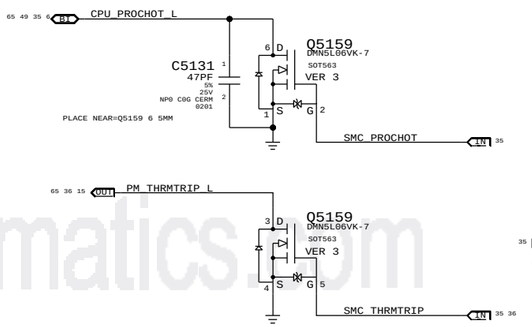
SMC Crystal Circuit

SMC USB Clock require these crystal values:5,6,8,10,12,16,18,20,24,25 MHz

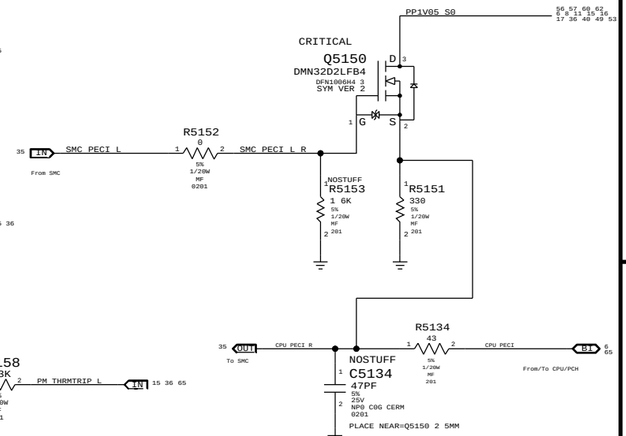


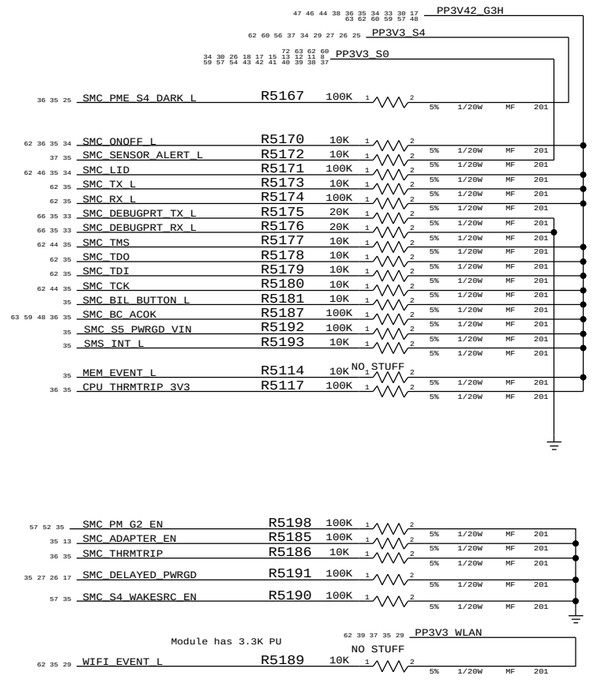






SMC12 PECI Support





SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: SMC Shared Support

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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39 37 35 SMC_HS_COMPUTING_ISENSE — SMC_HS_COMPUTING_ISENSE 35 37 39
MAKE BASE=TRUE

40 37 35 SMC_PBUS_VSENSE — SMC_PBUS_VSENSE 35 37 40
MAKE BASE=TRUE

39 37 35 SMC_BMON_ISENSE — SMC_BMON_ISENSE 35 37 39
MAKE BASE=TRUE

39 37 35 SMC_DCIN_ISENSE — SMC_DCIN_ISENSE 35 37 39
MAKE BASE=TRUE

40 37 39 SMC_DCIN_VSENSE — SMC_DCIN_VSENSE 35 37 40
MAKE BASE=TRUE

41 37 35 SMC_BMON_DISCRETE_ISENSE — SMC_BMON_DISCRETE_ISENSE 35 37 41
MAKE BASE=TRUE

40 37 35 SMC_CPU_ISENSE — SMC_CPU_ISENSE 35 37 40
MAKE BASE=TRUE

39 37 35 SMC_OTHER_HI_ISENSE — SMC_OTHER_HI_ISENSE 35 37 39
MAKE BASE=TRUE

41 37 35 SMC_PANEL_ISENSE — SMC_PANEL_ISENSE 35 37 41
MAKE BASE=TRUE

39 37 35 SMC_1V2S3_ISENSE — SMC_1V2S3_ISENSE 35 37 39
MAKE BASE=TRUE

39 37 35 SMC_LCDBKLT_ISENSE — SMC_LCDBKLT_ISENSE 35 37 39
MAKE BASE=TRUE

40 37 35 SMC_P3V3S5_ISENSE — SMC_P3V3S5_ISENSE 35 37 40
MAKE BASE=TRUE

39 37 35 SMC_WLAN_ISENSE — SMC_WLAN_ISENSE 35 37 39
MAKE BASE=TRUE

39 37 35 SMC_SSD_ISENSE — SMC_SSD_ISENSE 35 37 39
MAKE BASE=TRUE

39 37 35 SMC_P3V3S0_ISENSE — SMC_P3V3S0_ISENSE 35 37 39
MAKE BASE=TRUE

39 37 35 SMC_CAMERA_ISENSE — SMC_CAMERA_ISENSE 35 37 39
MAKE BASE=TRUE

NC_SMC_ADC16 — OUT 35 63 SD alias on page 103

40 37 35 SMC_P1V05S0_VSENSE — SMC_P1V05S0_VSENSE 35 37 40
MAKE BASE=TRUE

40 37 35 SMC_CPUDDR_ISENSE — SMC_CPUDDR_ISENSE 35 37 40
MAKE BASE=TRUE

40 37 35 SMC_P1V05S0_ISENSE — SMC_P1V05S0_ISENSE 35 37 40
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40 37 35 SMC_CPU_VSENSE — SMC_CPU_VSENSE 35 37 40
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41 37 35 SMC_CPU_IMON_ISENSE — SMC_CPU_IMON_ISENSE 35 37 41
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62 39 37 36 35 29 PP3V3_WLAN — PP3V3_WLAN 29 35 36 37 39 62
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SMC_SENSOR_PWR_EN 35 37 40 56

56 40 37 35 SMC_SENSOR_PWR_EN 35 37 40 56
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37 35 29 SMC_WIFI_PWR_EN — SMC_WIFI_PWR_EN 29 35 37
MAKE BASE=TRUE

37 35 TP_SMC_5VSW_PWR_EN — TP_SMC_5VSW_PWR_EN 35 37
MAKE BASE=TRUE

35 IN SMC_PCH_SUSWARN_L — R5230 0 5% 1/20W MF 0201 — PCH_SUSWARN_L OUT 13
MAKE BASE=TRUE

35 OUT SMC_PCH_SUSACK_L — R5231 0 5% 1/20W MF 0201 — PCH_SUSACK_L IN 13
MAKE BASE=TRUE

Top-Block Swap

PP3V3_S0 — R5296 1K 5% 1/20W MF 201 — R5283 1K 5% 1/20W MF 201
62 63 72 8 11 12 13 15 17 18 26 30 34 36 38 39 40 41 42 43 54 57 59 60

35 IN SMC_TOPBLK_SWP_L — PCH_STRP_TOPBLK_SWP_L OUT 15

62 60 56 37 36 34 29 27 26 25 PP3V3_S4

37 35 29 SMC_WIFI_PWR_EN — R5295 10K NOSTUFF 5% 1/20W MF 201

56 40 37 35 SMC_SENSOR_PWR_EN — R5294 10K NOSTUFF 5% 1/20W MF 201

PP3V3_S4 — R5282 100K 5% 1/20W MF 201
25 26 27 29 34 36 37 56 60 62

35 34 29 37 IN SMC_PME_S4_WAKE_L
35 34 29 37 IN SMC_PME_S4_WAKE_L — SMC_PME_S4_WAKE_L OUT 29 34 35 37
MAKE BASE=TRUE

41 IN SMC_HS_COMP_ALERT_L — R5216 100 5% 1/20W MF 201

18 14 IN PCH_SML1ALERT_L — NOSTUFF R5215 100 5% 1/20W MF 201

41 IN SMC_BMON_COMP_ALERT_L — R5213 100 5% 1/20W MF 201

63 59 IN FINSTACKSNS_ALERT_L — R5210 100 5% 1/20W MF 201

42 IN CPUTHMSNS_ALERT_L — R5214 100 5% 1/20W MF 201

42 IN CPUBMONSNS_ALERT_L — NOSTUFF R5211 100 5% 1/20W MF 201

42 IN TBTMLBSNS_ALERT_L — R5212 100 5% 1/20W MF 201 — SMC_SENSOR_ALERT_L OUT 35 36

SYNC_MASTER=J43_MLB SYNC_DATE=02/20/2013

PAGE TITLE
SMC Project Support

Apple Inc.

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REVISION <E4LABEL>
BRANCH <BRANCH>
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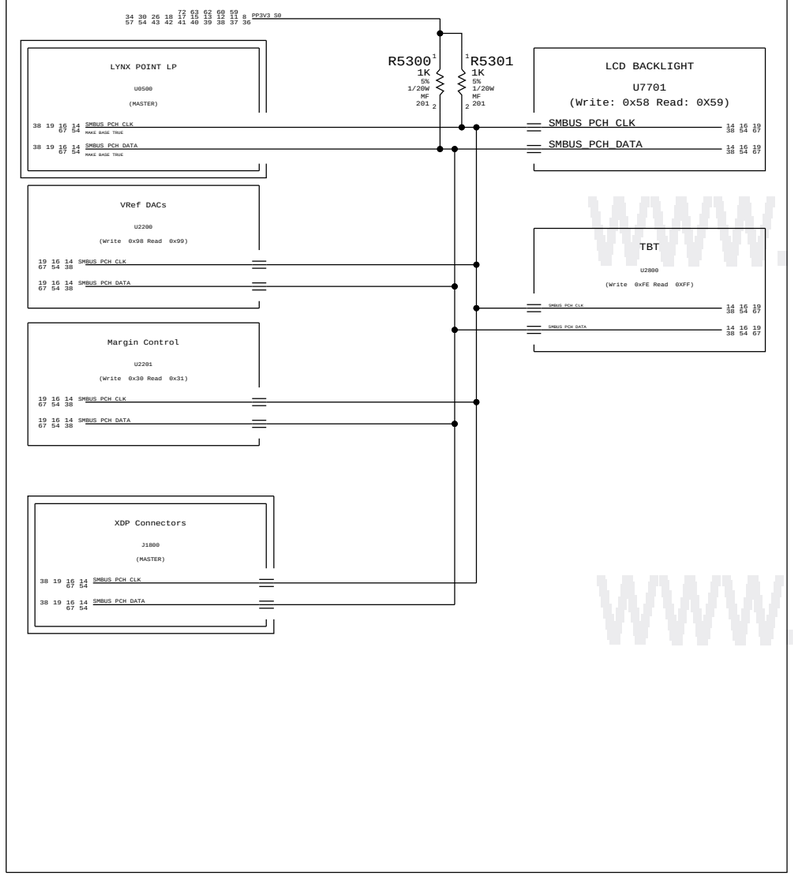
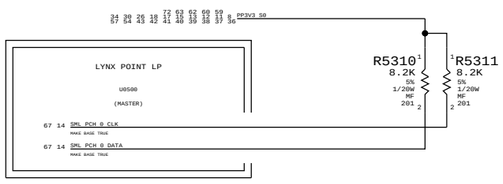
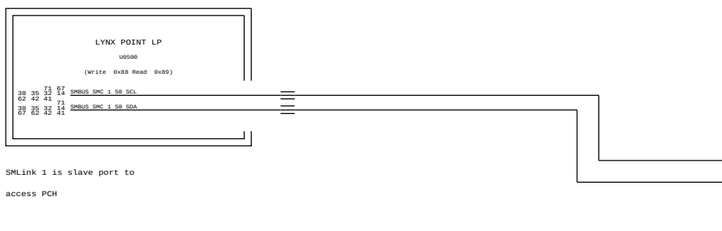
LYNX POINT LP S0 SMBus "0" Connections



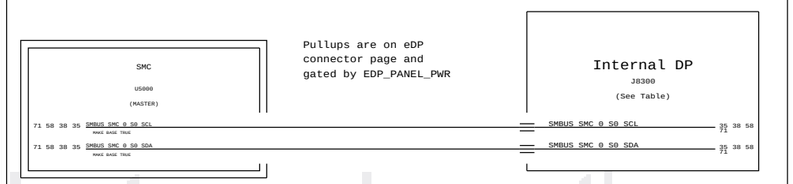
LYNX POINT LP S0 "SMLink 0" Connections



LYNX POINT LP S0 "SMLink 1" Connections



SMC "0" SMBus S0 Connections

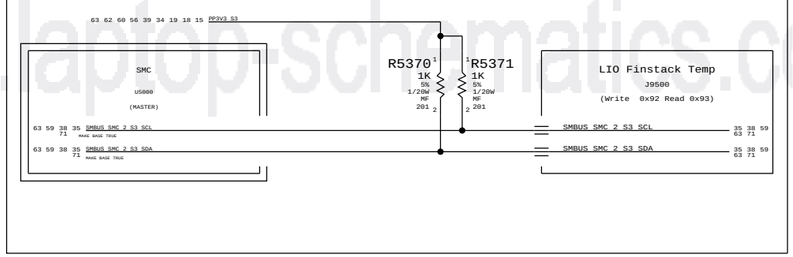


(* = Multiple options)

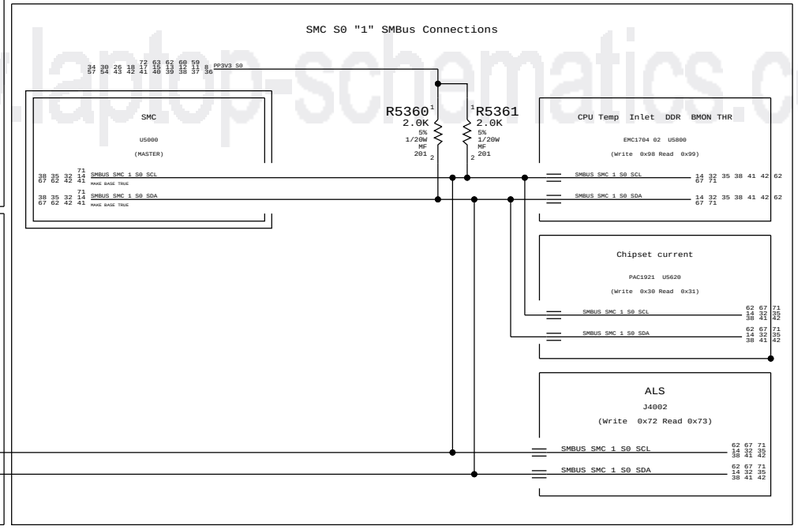
Internal DP

		J43 Samsung	J43 LGD	J43 Samsung	J41 LGD	J41 AUO
Analogix T con	(Write 0x7B/0x87 Read 0x7C/0x8B)	N	Y	*	Y	*
Parade T con	(0x10 0x1F or 0x30 0x3F)	Y	N	*	N	*
DVR	(Write 0x4E Read 0x4F)	Y	Y	*	Y	N

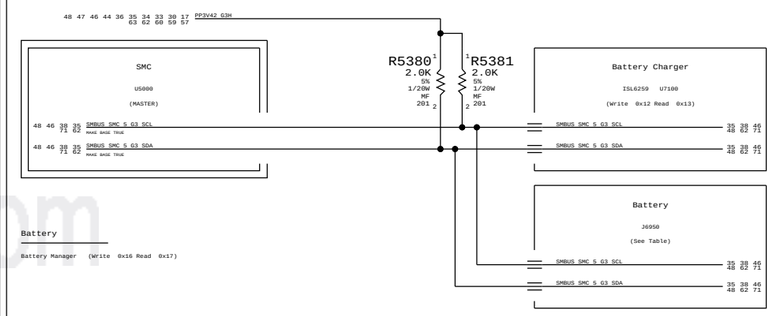
SMC "2" SMBus S3 Connections



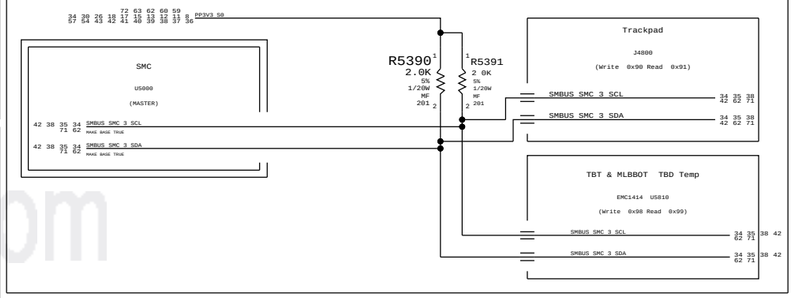
SMC S0 "1" SMBus Connections



SMC "5" SMBus G3H Connections



SMC "3" SMBus S0 Connections



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PAGE TITLE

SMBus Connections

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

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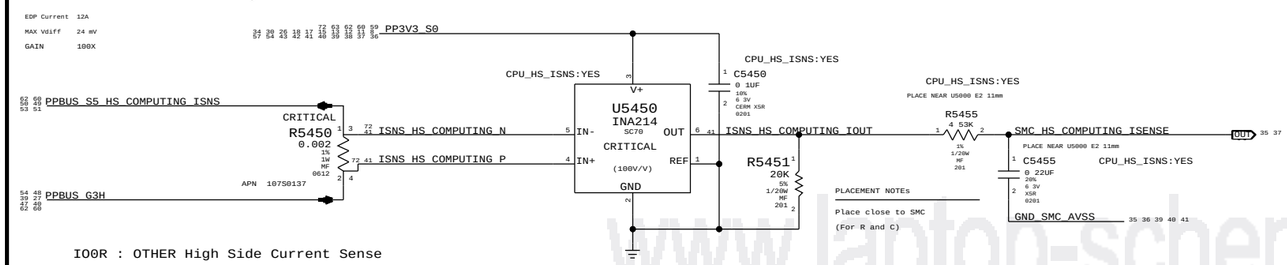
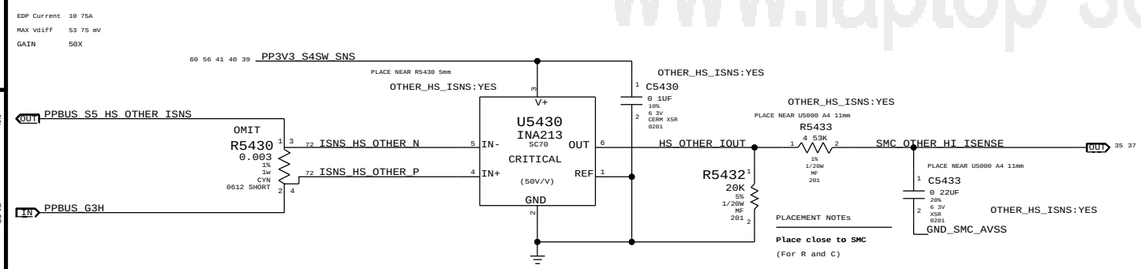
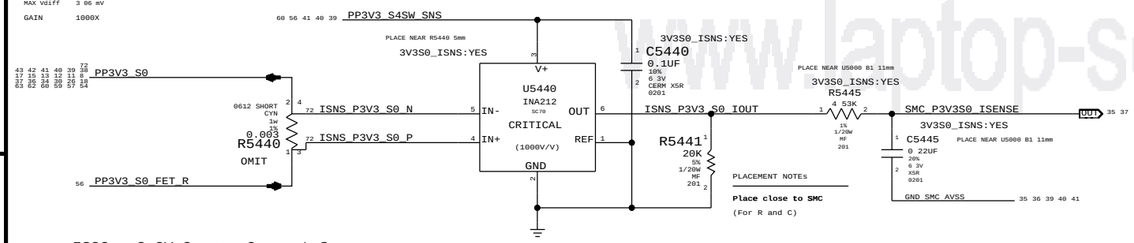
IC0R : COMPUTING High Side Current Sense



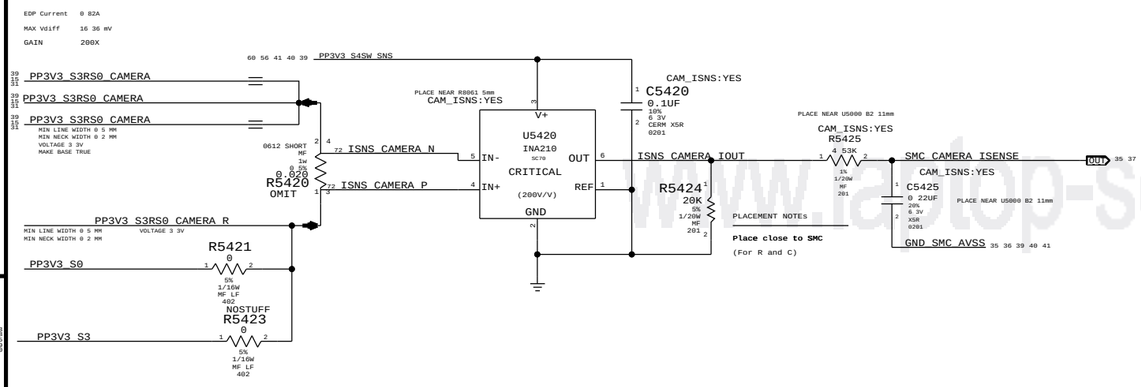
IO0R : OTHER High Side Current Sense



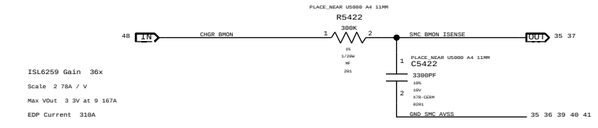
IR0C : 3.3V S0 FET Current Sense



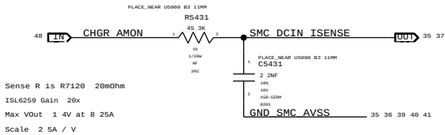
IS2C : 3.3V Camera Current Sense



CHARGER BMON High Side Current Sense

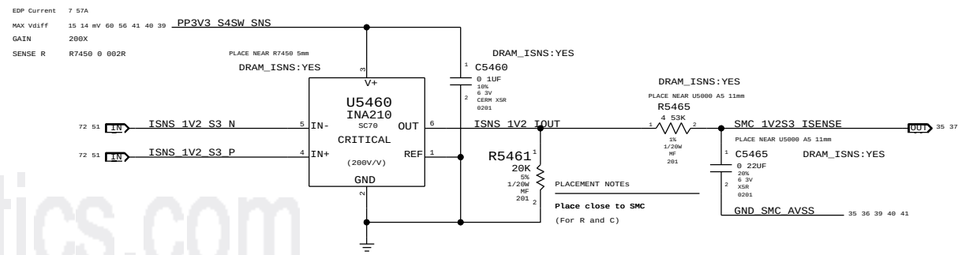


DC-IN (AMON) Current Sense

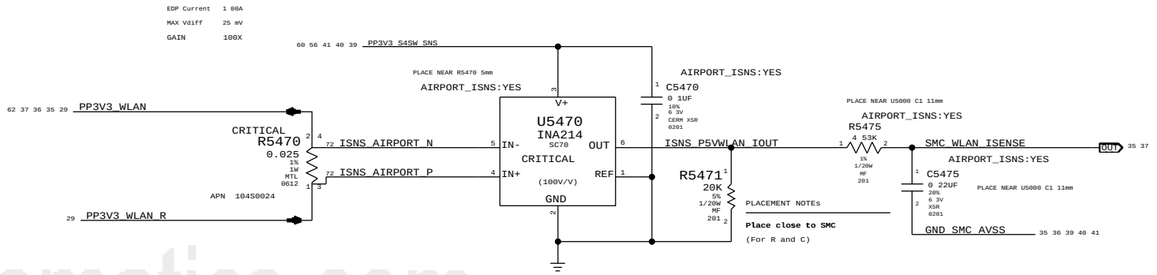


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
107S0248	1	RES SENSE 0 003OHM 1W 4 TERM 1% 0612 TFT	R5480	CRITICAL	

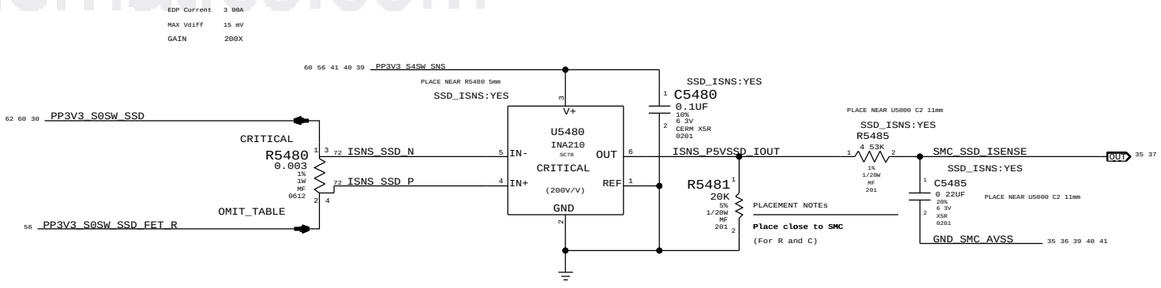
IM3C :DDR 1V2 Current Sense (LPDDR + CPUDDR)



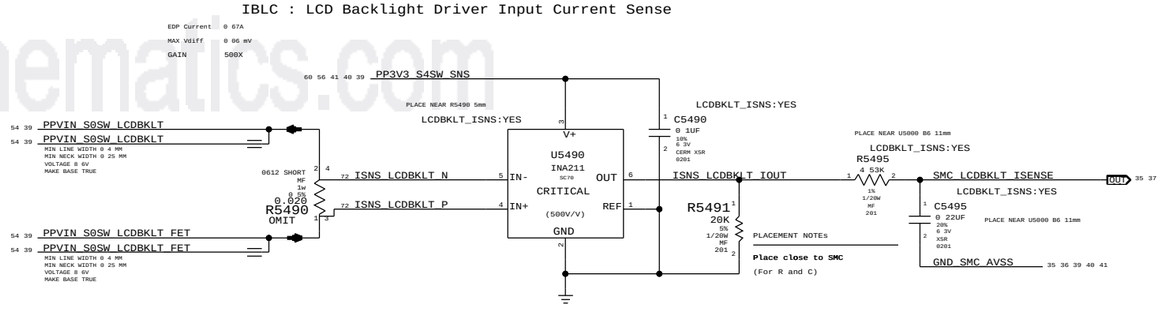
IAPC :AirPort Current Sense



ISDC : SSD Current Sense



IBLC : LCD Backlight Driver Input Current Sense



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5455		CPU HS ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5465		DRAM ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5475		AIRPORT ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5485		SSD ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5495		LCDBKLT ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5433		OTHER HS ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5425		CAM ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5445		3V3S0 ISNS NO

SYNC_MASTER=SID_J41 SYNC_DATE=02/26/2013

PAGE TITLE: High Side Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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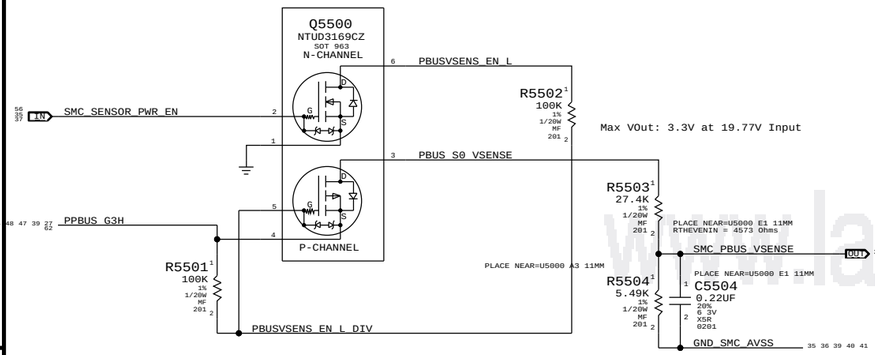
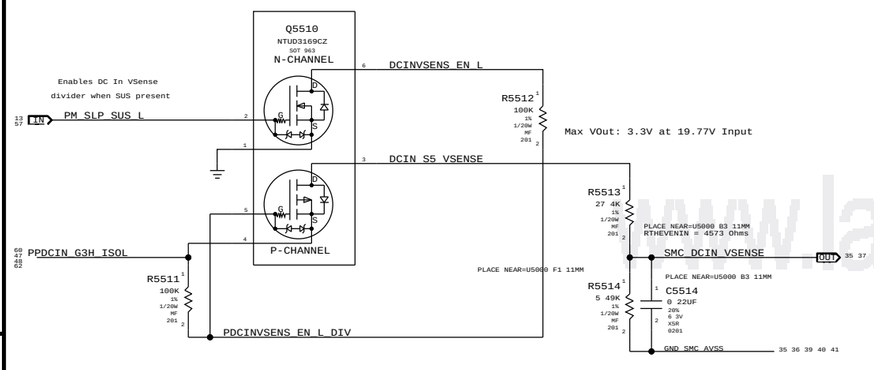
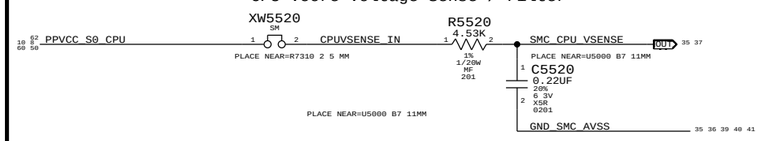
VP0R: PBUS Voltage Sense Enable & Filter



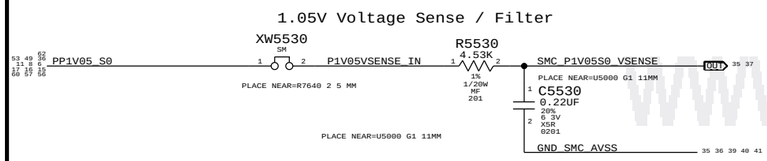
VD0R: DC-In Voltage Sense Enable & Filter



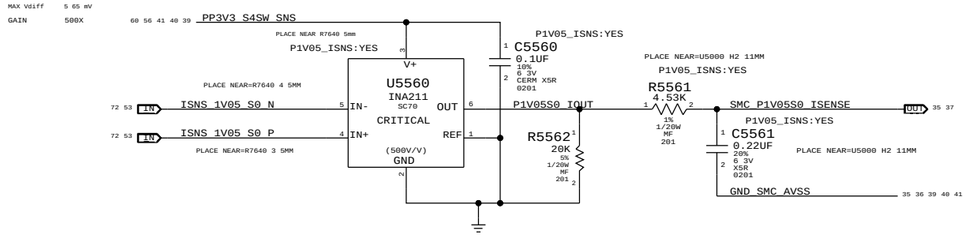
CPU Vcore Voltage Sense / Filter



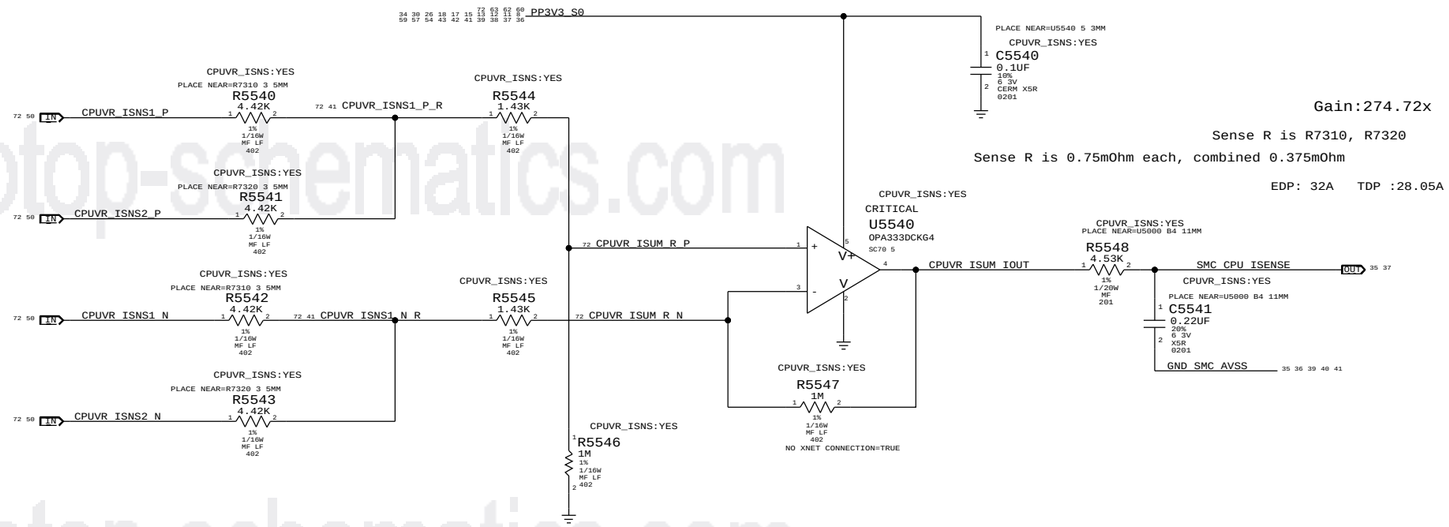
1.05V Voltage Sense / Filter



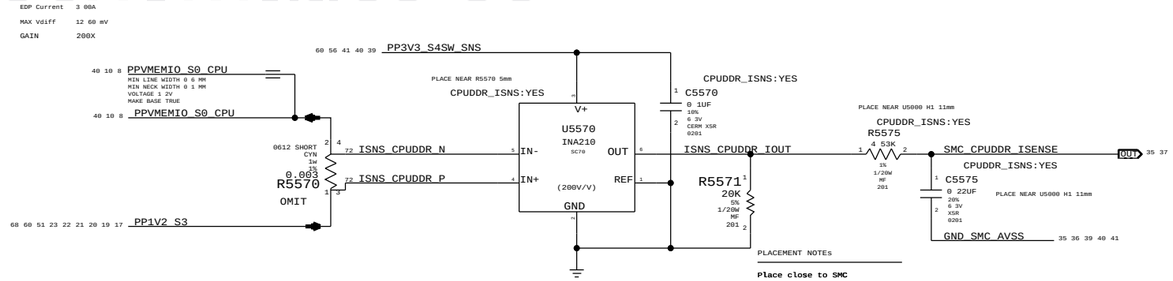
IC1C: 1.05V S0 CURRENT SENSE / FILTER



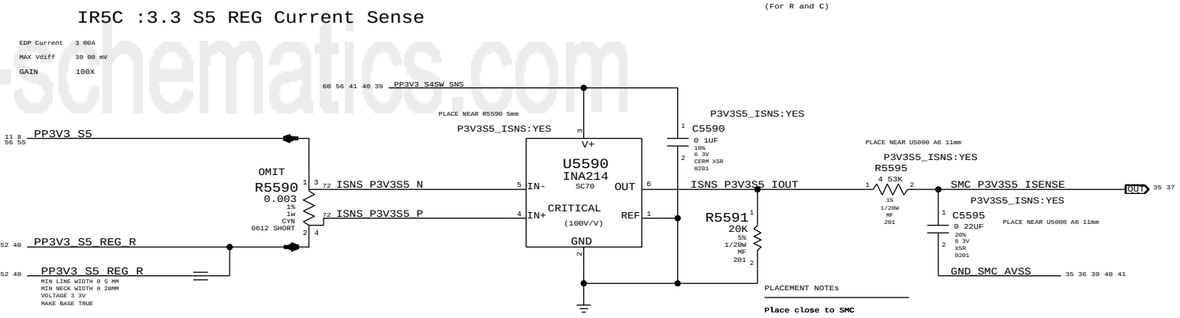
ICS0 : CPU VCore Load Side Current Sense



IM0C : CPU DDR Current Sense



IR5C :3.3 S5 REG Current Sense



Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5541		CPUVR ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5561		P1V05 ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5595		P3V3S5 ISNS NO
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5575		CPUDDR ISNS NO

SYNC_MASTER=SID_J41 SYNC_DATE=02/26/2013

PAGE TITLE
Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
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ICS3 : Adjustable Gain CPU VR Current

PP3V3_S4SW_SNS → R5620 100 1% 1/16W MF LF 402 → PP3V3_SNS_CPUVR_ADJUST_ISNS

C5620 1.0UF 20% 6.3V X5R 0201 1

MIN LINE WIDTH 0.5 mm
MIN NECK WIDTH 0.20 mm
VOLTAGE 3.3V

R5821: ADDR - 0x56/0x57 (r/w)

R5621 4.3K 5% 1/20W MF 201 — CPUVRSNS_ADDR_SEL

BYPASS=U5620 1 5 3MM

U5620 PAC1921-1-AIA DFN

	VDD		
ADDR_SEL/GAIN_SEL		OUT	SMC_CPUVR_ADJUST_ISENSE_R
IN CPUVR_ISNS1_P_R	SENSE+	READ*/INT	SMC_CPU_DBGPWR_RD_L → IN 35
IN CPUVR_ISNS1_N_R	SENSE-	SM_CLK/INT_SEL	SMBUS_SMC_1_S0_SCL → BI 14 32 35 37 42 62 67 71
		SM_DATA/OUT_SEL	SMBUS_SMC_1_S0_SDA → BI 14 32 35 38 42 62 67 71
		COMM_SEL	
GND	EPAD		

PLACE_NEAR=U5540 1 5MM

PU: SMBus mode

PLACE_NEAR=U5000 A7 5MM

R5625 0 5% 1/20W MF 0201 → SMC_CPUVR_ADJUST_ISENSE → OUT 35 37

C5625 0.22UF 20% 6.3V X5R 0201 — NO STUFF

GND_SMC_AVSS 35 36 39 40 41

Sense Pins gain stage for U5800 (EMC1704)

PP3V3_S0 → R5660 0 5% 1/20W MF 0201

PLACE_NEAR=U5660 3 5MM

C5660 0.1UF 10% 6.3V CERM X5R 0201

PLACE_NEAR=R7150 5MM

U5660 INA211 SC70 CRITICAL (500V/V)

	V+		
IN CKPLUS_WAIVE=NdifPr_badTerm	IN-	OUT	ISNS_HS_GAIN_OUT
IN CKPLUS_WAIVE=NdifPr_badTerm	IN+	REF	GND
IN ISNS_HS_COMPUTING_N			

R5663 20K 5% 1/20W MF 201

R5665 0 5% 1/20W MF 0201 — NO STUFF

C5665 0.22UF 20% 6.3V X5R 0201

R5666 0 5% 1/20W MF 0201 — ISNS_HS_GAIN_P_R → ISNS_HS_GAIN_P → OUT 42 72

R5662 1K 1% 1/20W MF 201 — IN ISNS_HS_COMPUTING_P

R5667 0 5% 1/20W MF 0201 — NO STUFF

R5668 0 5% 1/20W MF 0201 — ISNS_HS_GAIN_N_R → ISNS_HS_GAIN_N → OUT 42 72

R5661 27K 1% 1/20W MF 201 — IN ISNS_HS_COMPUTING_N

R5669 0 5% 1/20W MF 0201 — NO STUFF

GAIN: 500X

In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800.
This will set the minumum current threshold at 0.100mA

ILDC :LCD Panel Current Sense / Filter

PP3V3_S4SW_SNS

PP3V3_S0SW_LCD — MIN LINE WIDTH 0.3 MM, MIN NECK WIDTH 0.2 MM, VOLTAGE 3.3V, MAKE BASE TRUE

PP3V3_S0SW_LCD

OMIT R5670 0.020 0 5% 1W MF 0612 SHORT

ISNS_PANEL_N, ISNS_PANEL_P

PP3V3_S0SW_LCD_R — MIN LINE WIDTH 0.3 MM, MIN NECK WIDTH 0.2 MM, VOLTAGE 3.3V, MAKE BASE TRUE

PP3V3_S0SW_LCD_R

EDP Current 0 750 A
Max Vdiff 15 mV

PLACE_NEAR R5470 5mm — PANEL_ISNS:YES

U5670 INA210 SC70 CRITICAL (200V/V)

	V+		
ISNS_PANEL_N	IN-	OUT	ISNS_PANEL_IOUT
ISNS_PANEL_P	IN+	REF	GND

C5670 0.1UF 10% 6.3V CERM X5R 0201 — PANEL_ISNS:YES

PLACE_NEAR U5000 C1 11mm

R5675 4.53K 1% 1/20W MF 201 — PANEL_ISNS:YES → SMC_PANEL_ISENSE → OUT 35 37

C5675 0.22UF 6.3V X5R 0201 — PLACE_NEAR U5000 C1 11mm

GND_SMC_AVSS 35 36 39 40 41

R5671 20K 5% 1/20W MF 201

Gain: 200x
Scale 0.25A / V
MAX VOUT 3V AT 0.825A
PLACEMENT NOTES
Place close to SMC
(For R and C)

VR IMON Current Sense Filter

PLACE_NEAR U5000 B8 5MM

CPUVR_IMON → R5641 0 5% 1/20W MF 0201 → SMC_CPU_IMON_ISENSE → OUT 35 37

C5641 2.2NF 10% 16V X5R-CDM 0201 — NO STUFF, PLACE_NEAR U5000 B8 5MM

GND_SMC_AVSS 35 36 39 40 41

Vref = 0.406mV Vth = 0.442 = 1A from Battery
Vtl = 0.290mv = 0.687A from battery
Hysteresis TBD based on RC value changes

Discrete High side Current threshold

PP3V3_S0

C5613 0.1UF 10% 6.3V CERM X5R 0201 — BYPASS=U5601 3MM

R5614 294K 1% 1/16W MF LF 402

R5615 49.9K 1% 1/16W MF LF 402

R5616 10.2K 1% 1/16W MF LF 402 — HS_COMP_FB

HS_COMP_VREF

U5611 MCP6541T SC70-5 — HS_COMP_OUT

R5619 255K 1% 1/16W MF LF 402

C5611 0.22UF 20% 6.3V X5R 0201 — NO STUFF

HS_IOT_R

R5617 0 5% 1/20W MF 0201 — NOSTUFF

R5610 0 5% 1/20W MF 0201

C5610 0.1UF 10% 25V X5R 402 — NOSTUFF

HS_IOT_D

D5617 SM 201 RB521ZS-30 — NOSTUFF

39 IN ISNS_HS_COMPUTING_IOUT

U5612 DMN32D2LFB4 DFN1006H4 3 SYM VER 2 — SMC_HS_COMP_ALERT_L → OUT 37

Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

BMON : Discrete BMON Current Sense / Filter

PP3V3_S0

C5603 0.1UF 10% 6.3V CERM X5R 0201 — BYPASS=U5601 3MM

R5604 100K 1% 1/16W MF LF 402

R5605 100K 1% 1/16W MF LF 402 — BMON_COMP_VREF

R5606 10.2K 1% 1/16W MF LF 402 — BMON_COMP_FB

U5601 MCP6541T SC70-5

C5601 0.22UF 20% 6.3V X5R 0201 — NO STUFF

R5609 200K 1% 1/16W MF 402

BMON_COMP_OUT

U5602 DMN32D2LFB4 DFN1006H4 3 SYM VER 2 — SMC_BMON_COMP_ALERT_L → OUT 37

BMON_IOT_R

C5600 0.1UF 10% 25V X5R 402 — NOSTUFF

R5600 0 5% 1/20W MF 0201

R5607 0 5% 1/20W MF 0201 — NOSTUFF

BMON_IOT_D

D5607 SM 201 RB521ZS-30 — NOSTUFF

BYPASS=U5600:3MM

C5606 0.1UF 10% 6.3V CERM X5R 0201

CHGR_CSO_R_P/N are swapped on purpose to measure power into the system

U5600 INA213 SC70 CRITICAL (50V/V)

	V+		
IN CKPLUS_WAIVE=NdifPr_badTerm CHGR_CSO_R_P	IN-	OUT	BMON_IOUT
IN CKPLUS_WAIVE=NdifPr_badTerm CHGR_CSO_R_N	IN+	REF	GND

R5601 20K 5% 1/20W MF 201

PLACE_NEAR=U5000.A3:5MM

R5608 4.53K 1% 1/20W MF 201 — SMC_BMON_DISCRETE_ISENSE → OUT 35 37

C5602 0.22UF 20% 6.3V X5R 0201 — PLACE_NEAR=U5000.A3:5MM

GND_SMC_AVSS 35 36 39 40

Replacing caps with 100K PD on ISENSE SMC inputs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES MF 1/20W 100K OHM 5 0201 SMD	C5675		PANEL ISNS NO

SYNC MASTER=SID_J41 SYNC DATE=02/26/2013

PAGE TITLE: Debug Sensors 1

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
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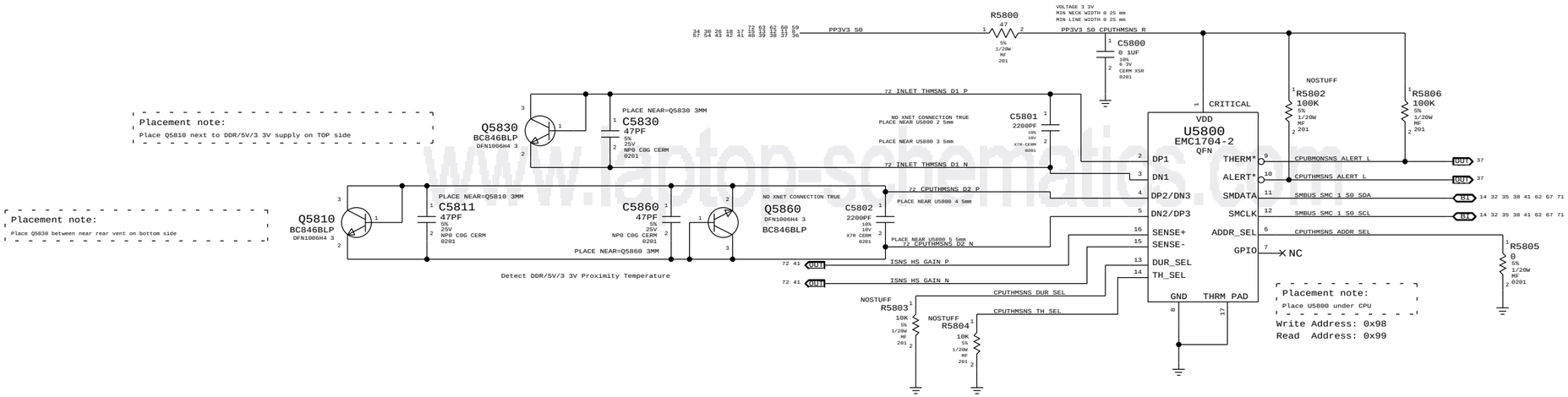
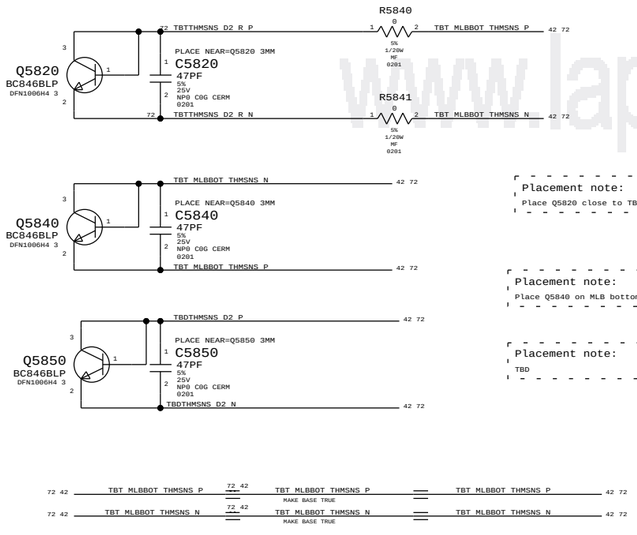
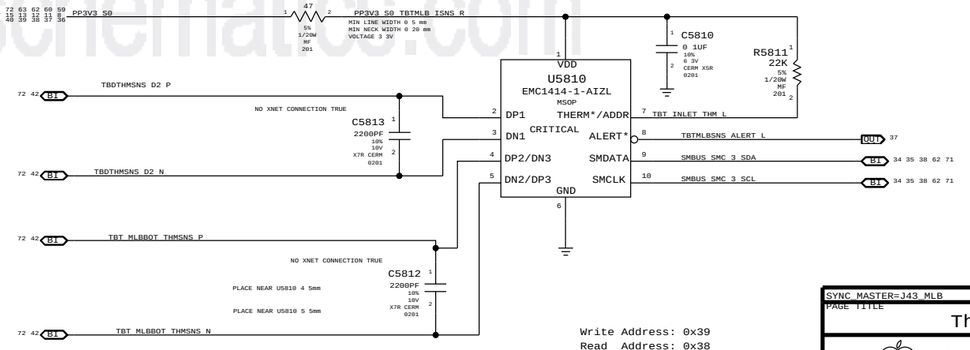
CPU Proximity, Inlet ,DDR and BMON THR Sensor



TBT,MLB Bottom Proximity Sensors



TBT, MLBBOT and TBD Temp Sensor



SYNC_MASTER=J43_MLB	SYNC_DATE=02/20/2013
PAGE TITLE	Thermal Sensors
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
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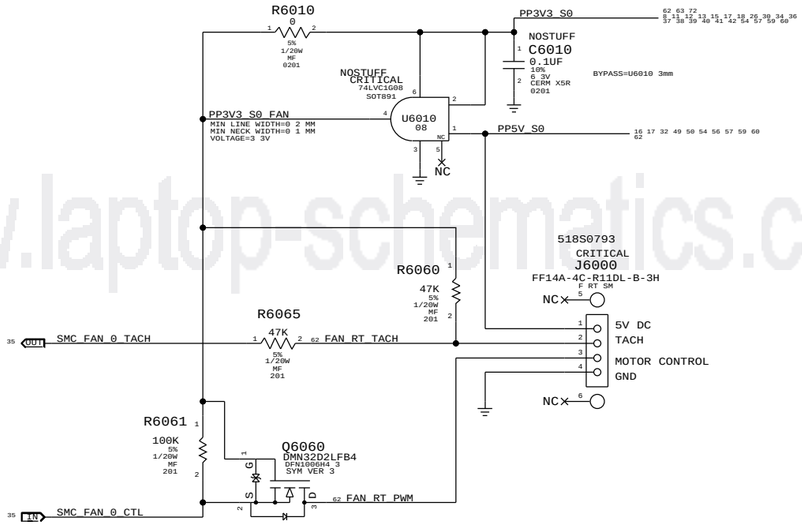
FAN CONNECTOR



SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE

Fan

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

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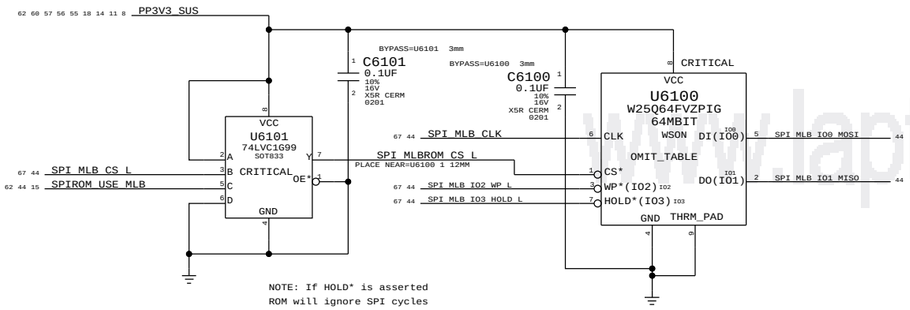
SPI ROM

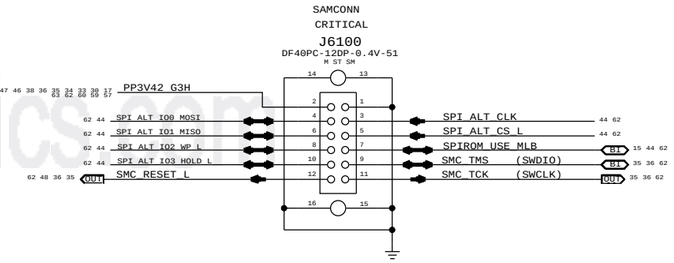
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



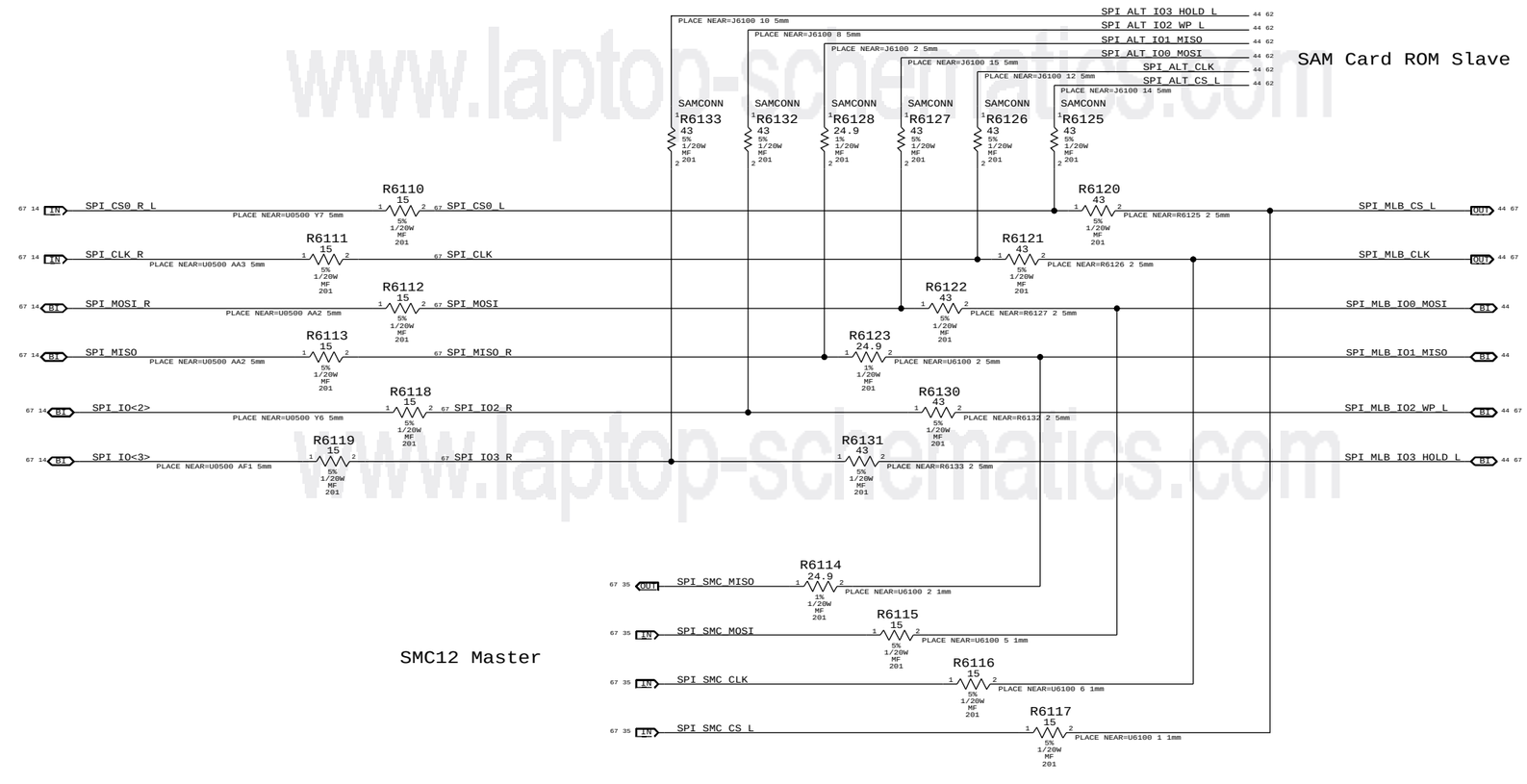
NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination



BOM_COST_GROUP=CPU SUPPORT

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/09/2013

PAGE TITLE: SPI Debug Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
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PAGE: 61 OF 120
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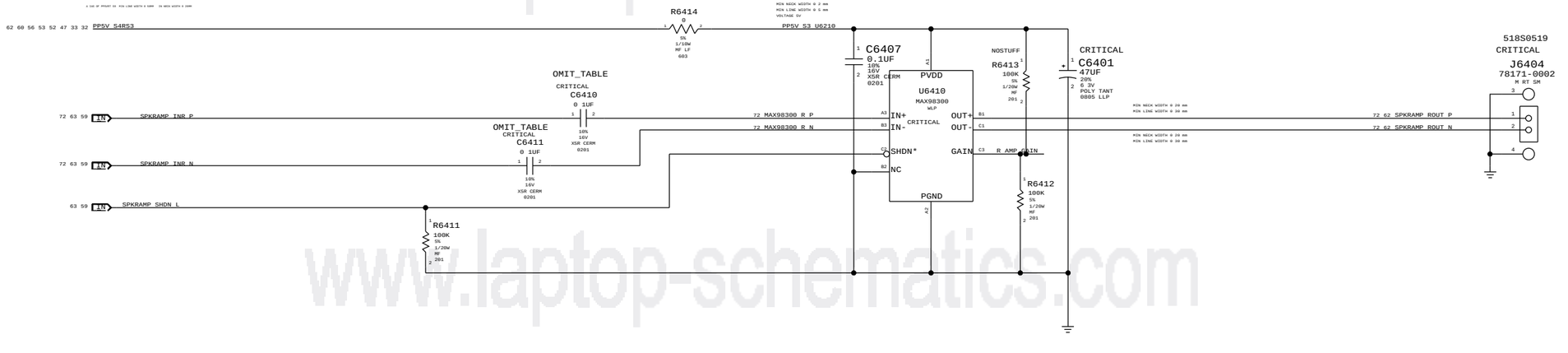
SPEAKER AMPLIFIERS

APN 353S2888

SPEAKER LOWPASS 80 HZ < FC < 132 HZ

GAIN 6DB



Right Speaker Connector

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
132S0460	2	CAP CER X5R 0 1UF 10% 16V 0201 MURATA	C6410,C6411	CRITICAL	

SYNC_MASTER=J43_MLB SYNC_DATE=09/04/2012

PAGE TITLE: Audio: Speaker Amp

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 64 OF 120

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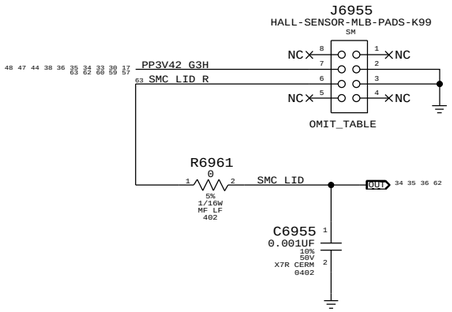
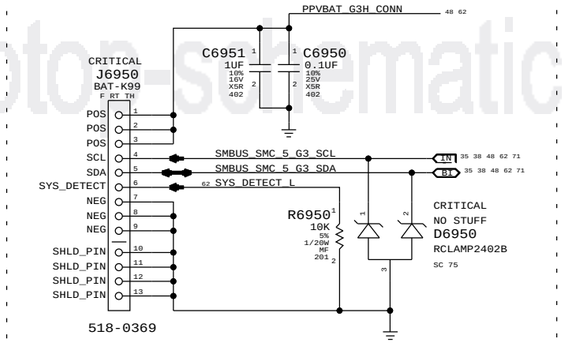
Hall Effect Sensor



11"-Specific

Battery Connector



SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

Battery Connector & Hall Effect

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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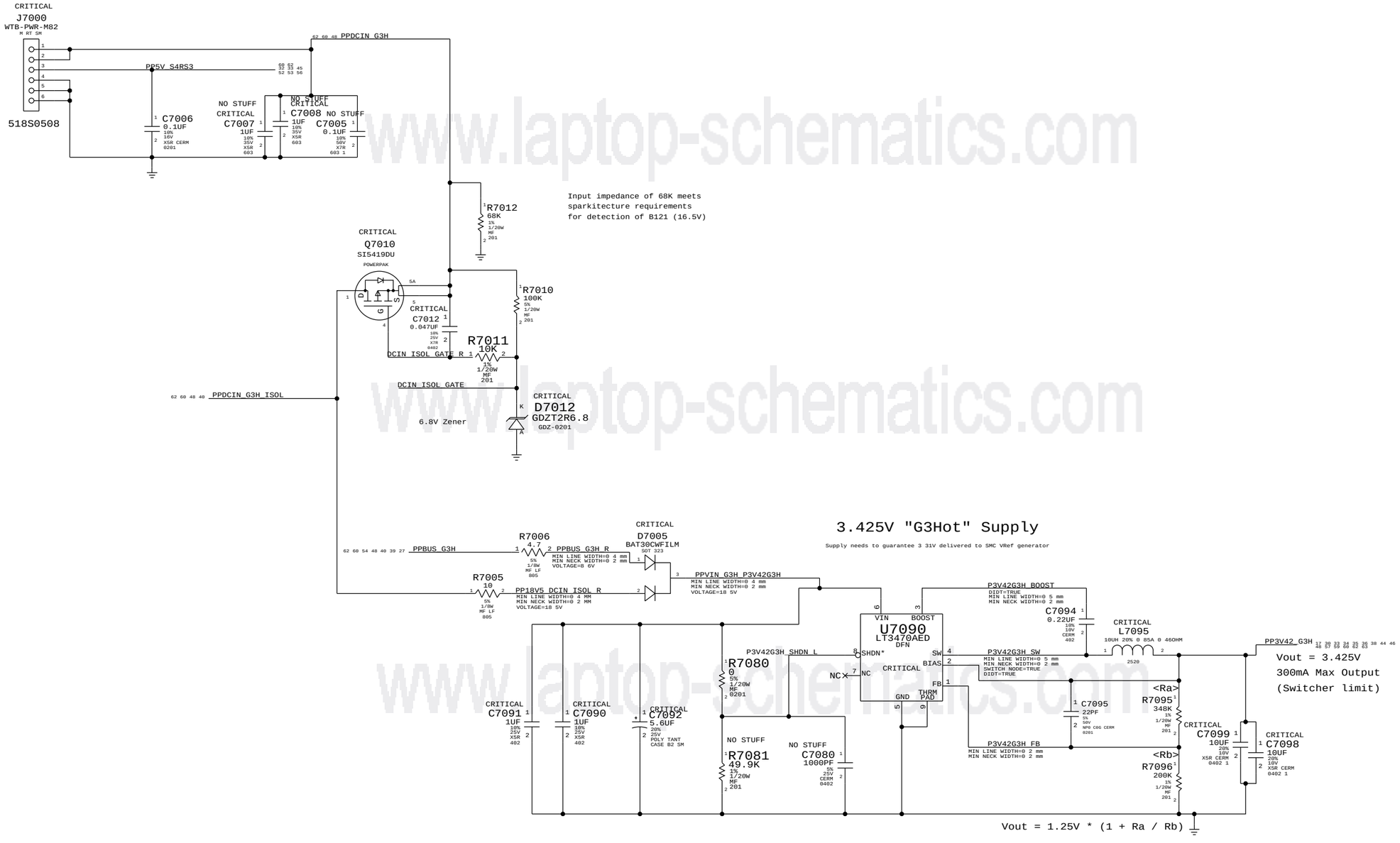
MLB to LIO Power Cable Connector



SYNC MASTER=J43 MLB SYNC DATE=09/13/2012

PAGE TITLE: DC-In & G3H Supply

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 70 OF 120

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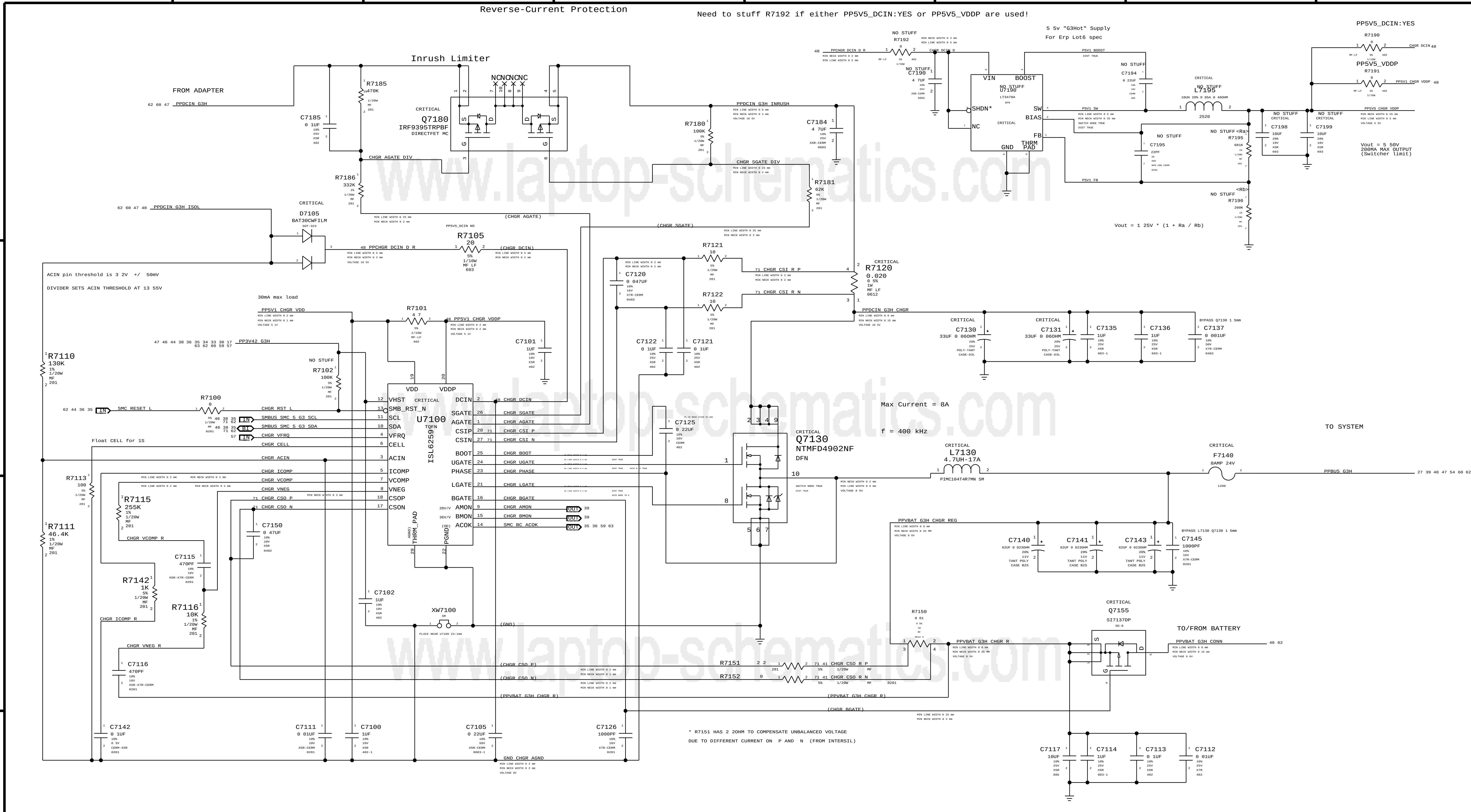

SYNC_MASTER=J43_MLB SYNC_DATE=09/14/2012

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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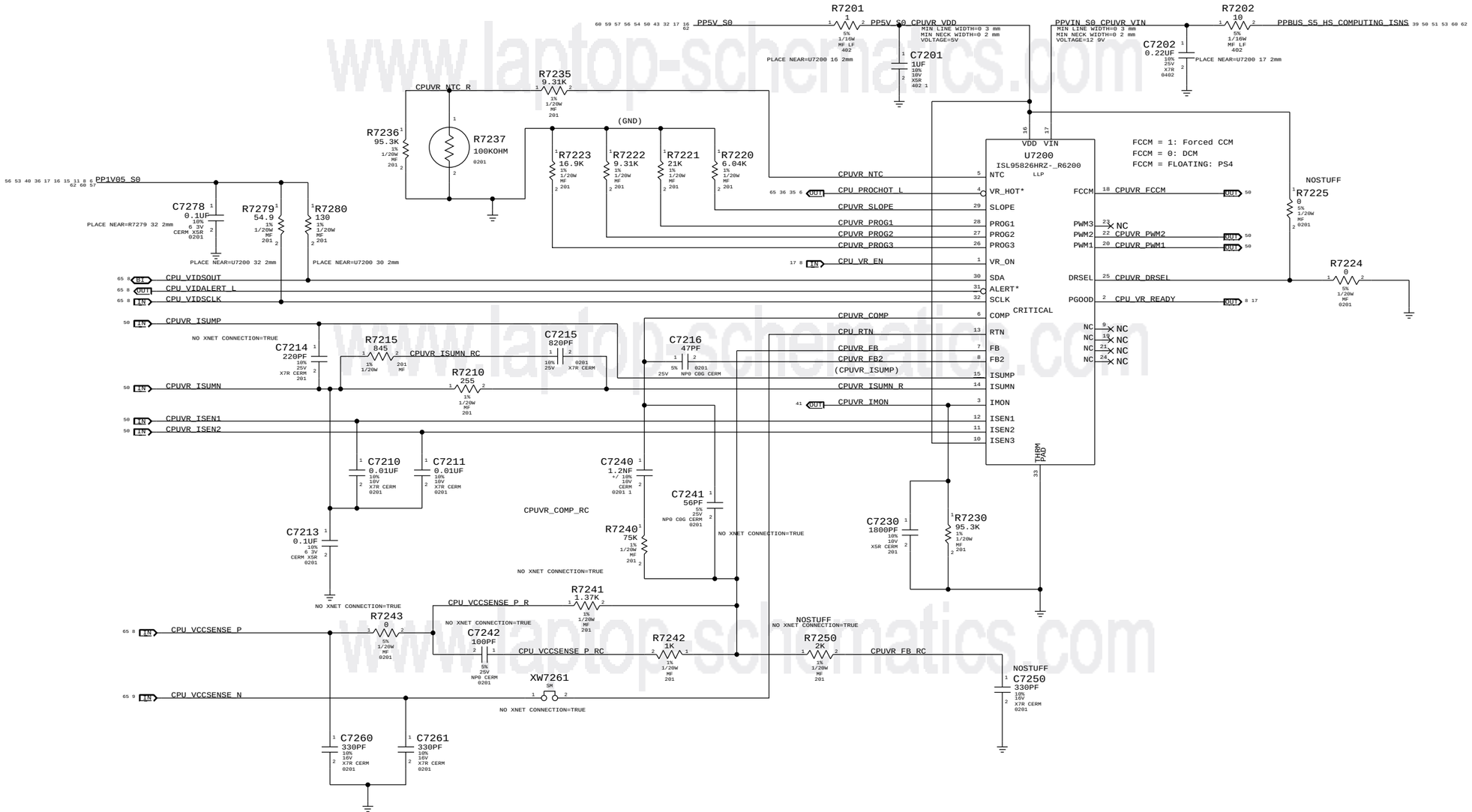

SYNC_MASTER=J43_MLB SYNC_DATE=10/09/2012

PAGE TITLE

CPU VR12.6 VCC Regulator IC

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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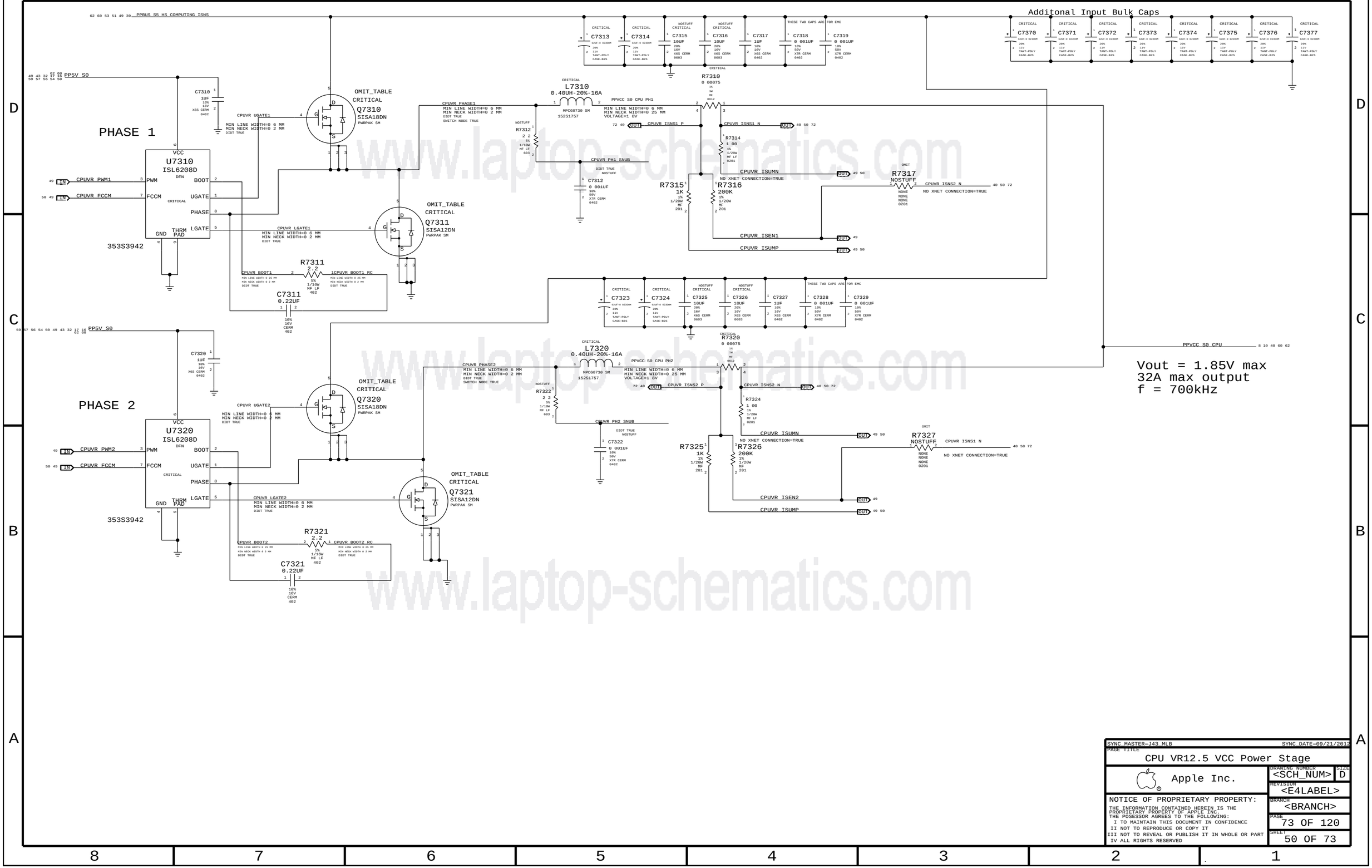

SYNC_MASTER=J43_MLB	SYNC_DATE=09/21/2012
PAGE TITLE: CPU VR12.5 VCC Power Stage	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
	PAGE: 73 OF 120
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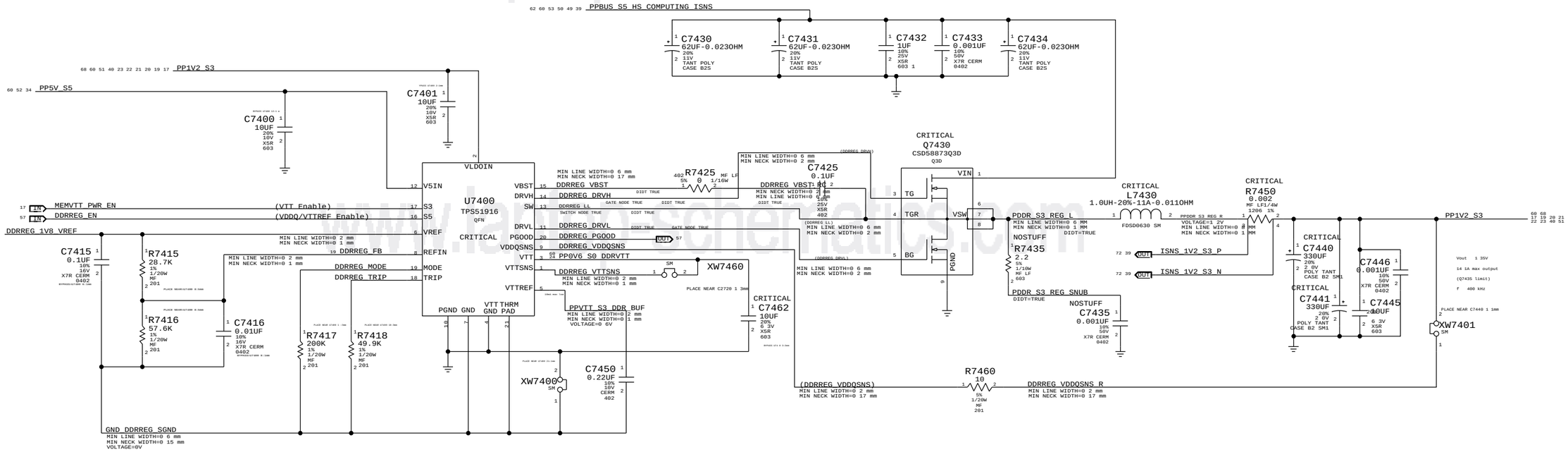

SYNC_MASTER=J43_MLB	SYNC_DATE=09/17/2012
PAGE TITLE	LPDDR3 Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
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SKIPSEL Strap	
VREF2	Auto Skip (Higher Efficiency)
VREG3	OOA Auto Skip (Lower Efficiency)

PPBUS_S5_HS_OTHER_ISNS

F=400KHZ

Vout = 5 0V

7 2A MAX OUTPUT

Vout = 3 3V

6 5A MAX OUTPUT

F=400KHZ

SYNC_MASTER=J43_MLB	SYNC_DATE=10/02/2012
PAGE TITLE: 5V S4RS3 / 3.3V S5 Power Supply	
Apple Inc.	DRAWING NUMBER: <SCH_NUM> SIZE: D
	REVISION: <E4LABEL>
	BRANCH: <BRANCH>
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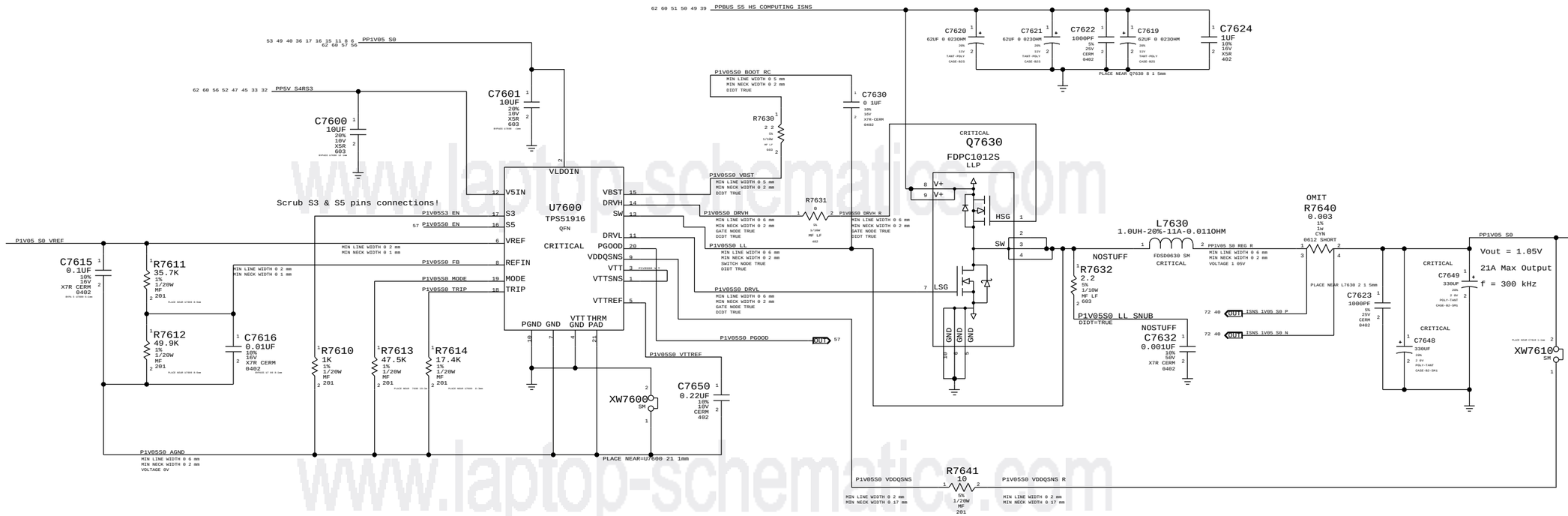
1.05V S0 Regulator



SYNC_MASTER=J43_MLB	SYNC_DATE=09/10/2012
PAGE TITLE	1.05V S0 Power Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
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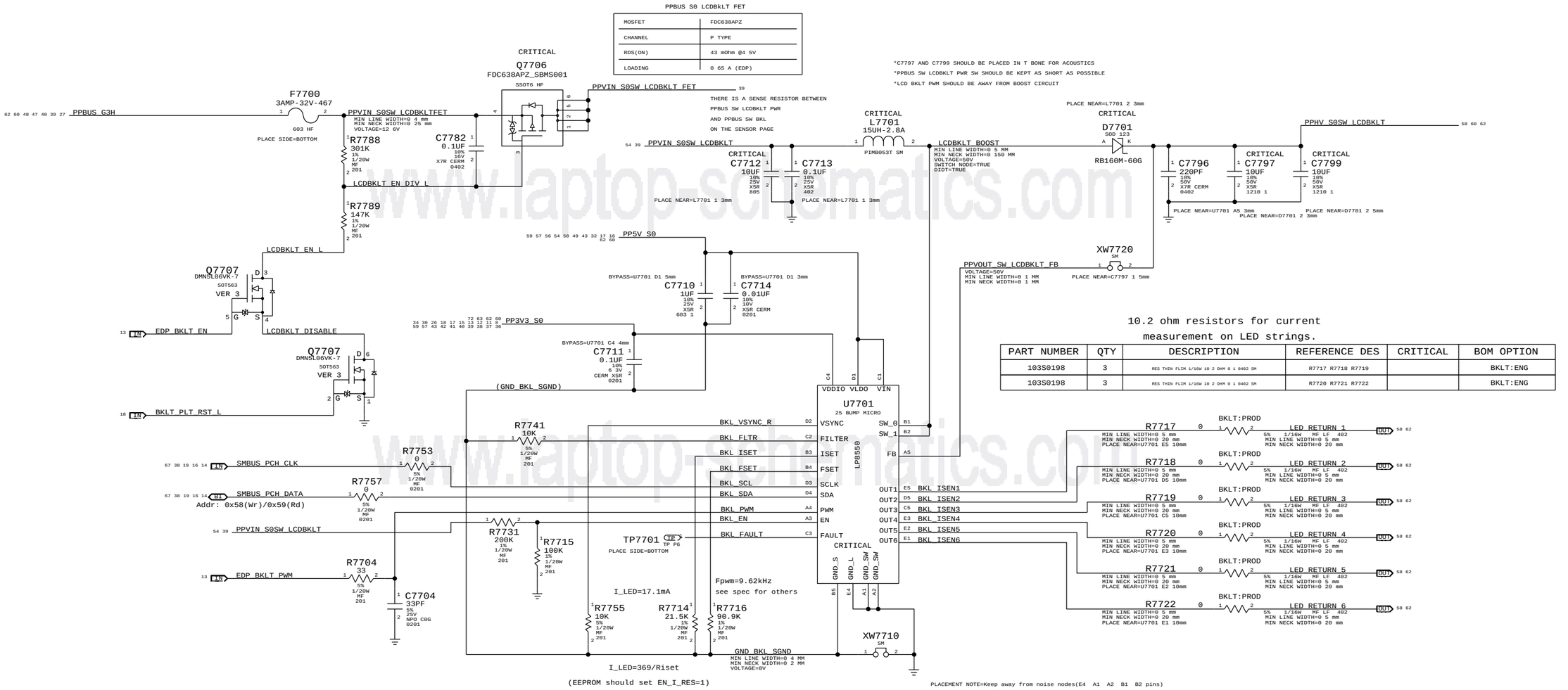

SYNC_MASTER=J43_MLB SYNC_DATE=09/13/2012

PAGE TITLE

LCD/KBD Backlight Driver

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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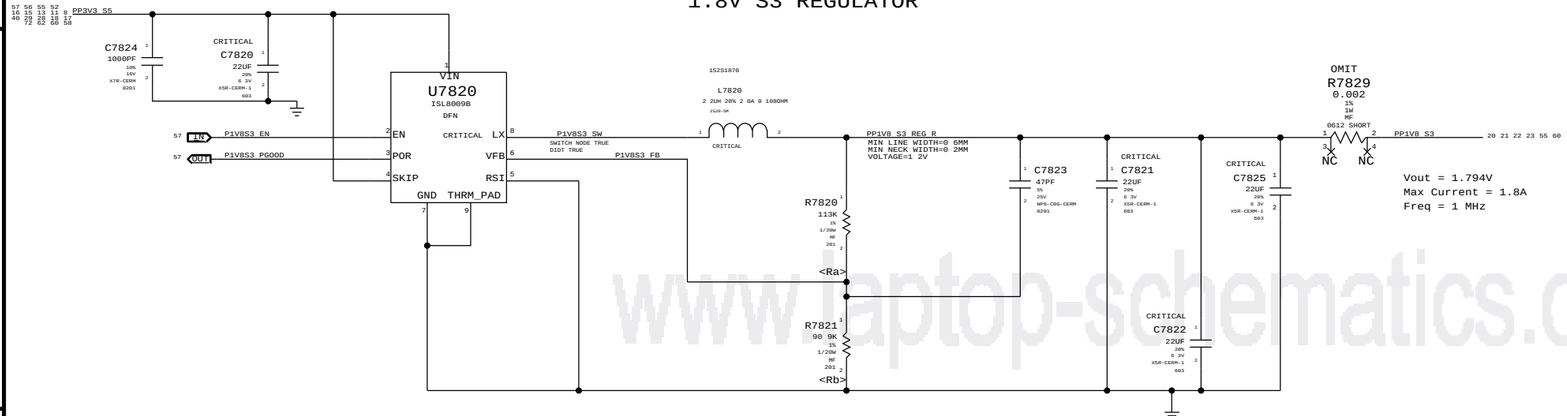
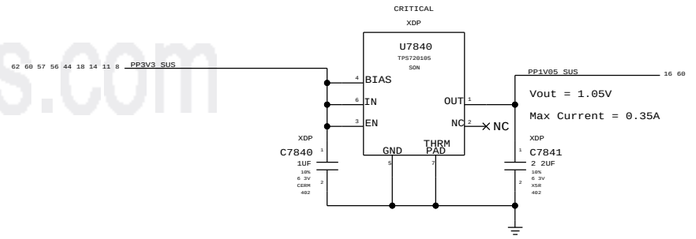
1.8V S3 REGULATOR

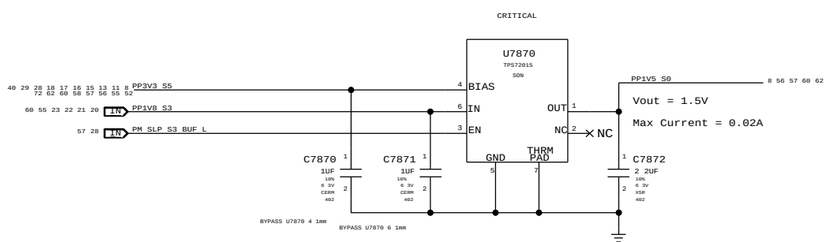


1.05V SUS LDO

Cougar Point requires JTAG pull ups to be powered at 1 05V when SUS suspend well is active
Pull ups (3) must be 51 ohms to support XDP (not required in production)
70mA is required to support pull ups Alternative is strong voltage
dividers (200/100) to 3 3V S5 which burns 100mW in all S states



1.5V S0 LDO



SYNC_MASTER=J43_MLB SYNC_DATE=10/04/2012

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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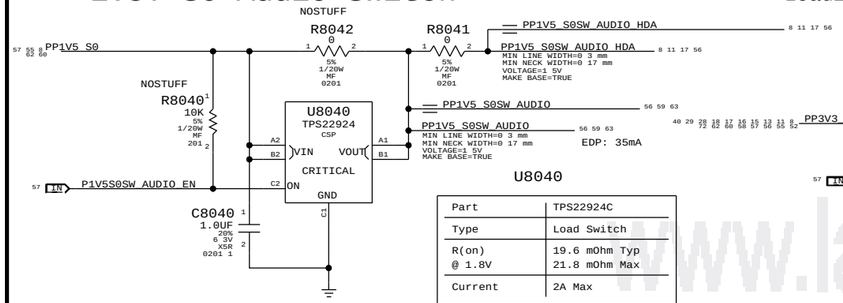
1.5V S0 Audio Switch

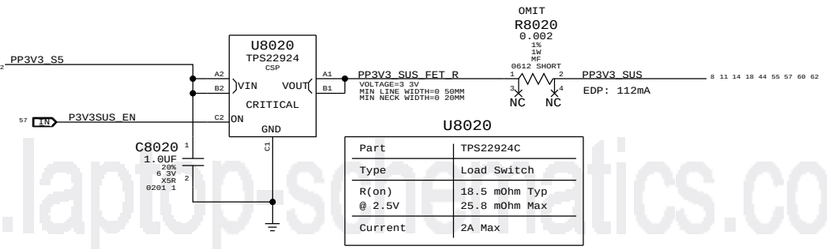
Loading specs per J41/43_PowerBudget_Riviera_rev0.99e



U8040

Part	TPS22924C
Type	Load Switch
R(on) @ 1.8V	19.6 mOhm Typ 21.8 mOhm Max
Current	2A Max

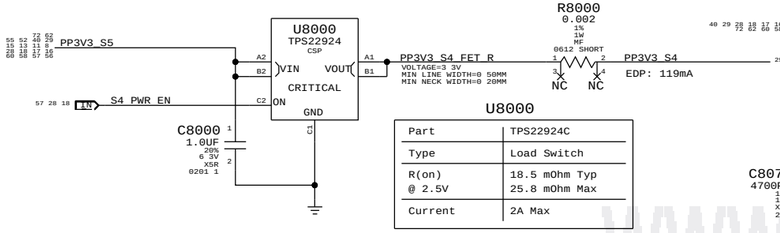
3.3V SUS Switch



U8020

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

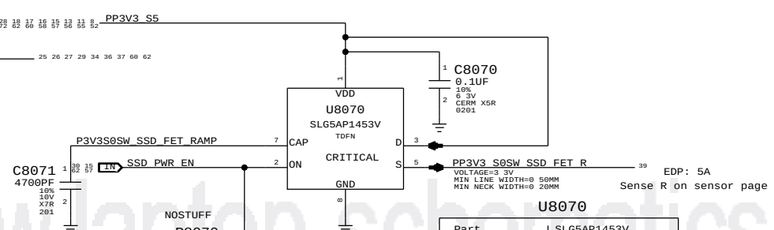
3.3V S4 Switch



U8000

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

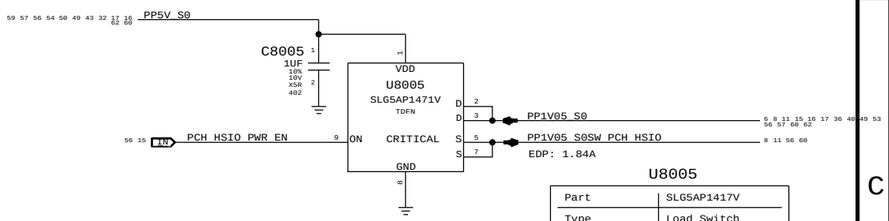
3.3V SSD Switch



U8070

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 25C	7.8 mOhm Typ 8.5 mOhm Max
Current	5.3A Max

1.05V PCH HSIO Switch

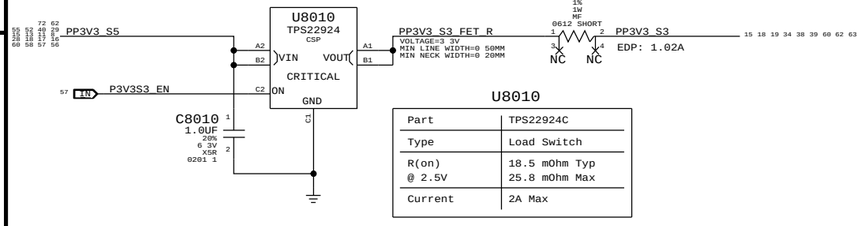


U8005

Part	SLG5AP1417V
Type	Load Switch
R(on) @ 4V Vgs	9.8 mOhm Typ TBD mOhm Max
Current	6A Max

HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

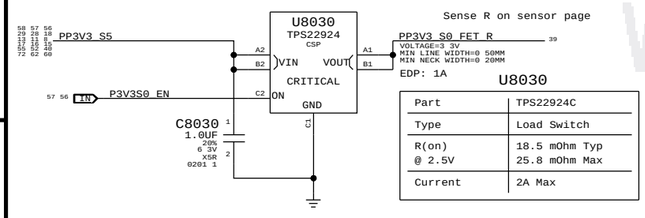
3.3V S3 Switch



U8010

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

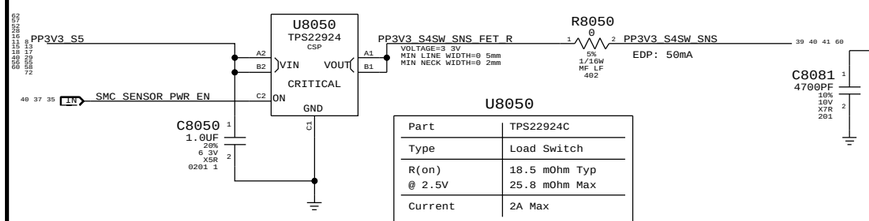
3.3V S0 Switch



U8030

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

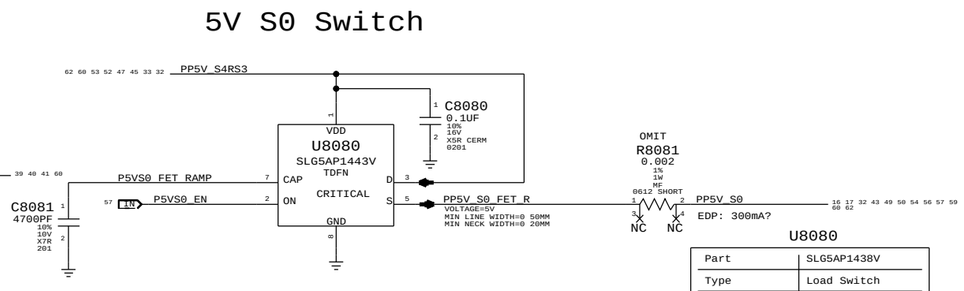
3.3V Sensor Switch



U8050

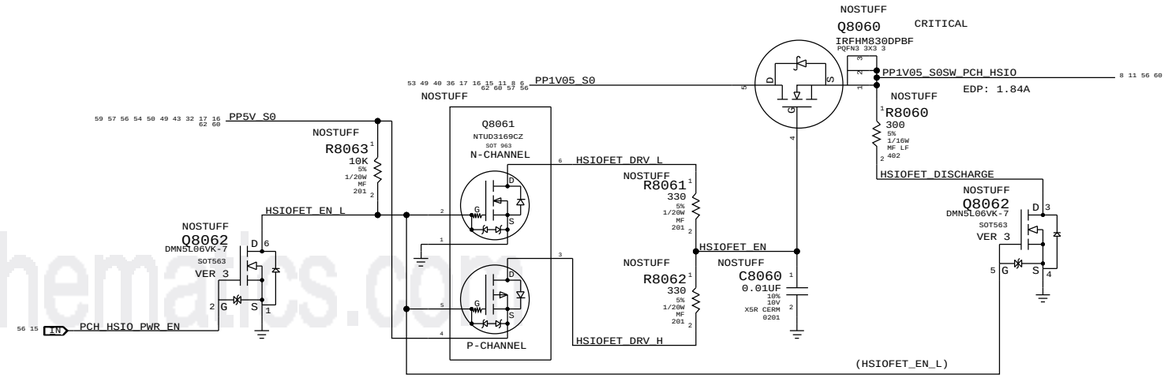
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max
Current	2A Max

5V S0 Switch



U8080

Part	SLG5AP1438V
Type	Load Switch
R(on)	15 mOhm Typ 17 mOhm Max
Current	2.5A



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	Apple Inc.
DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
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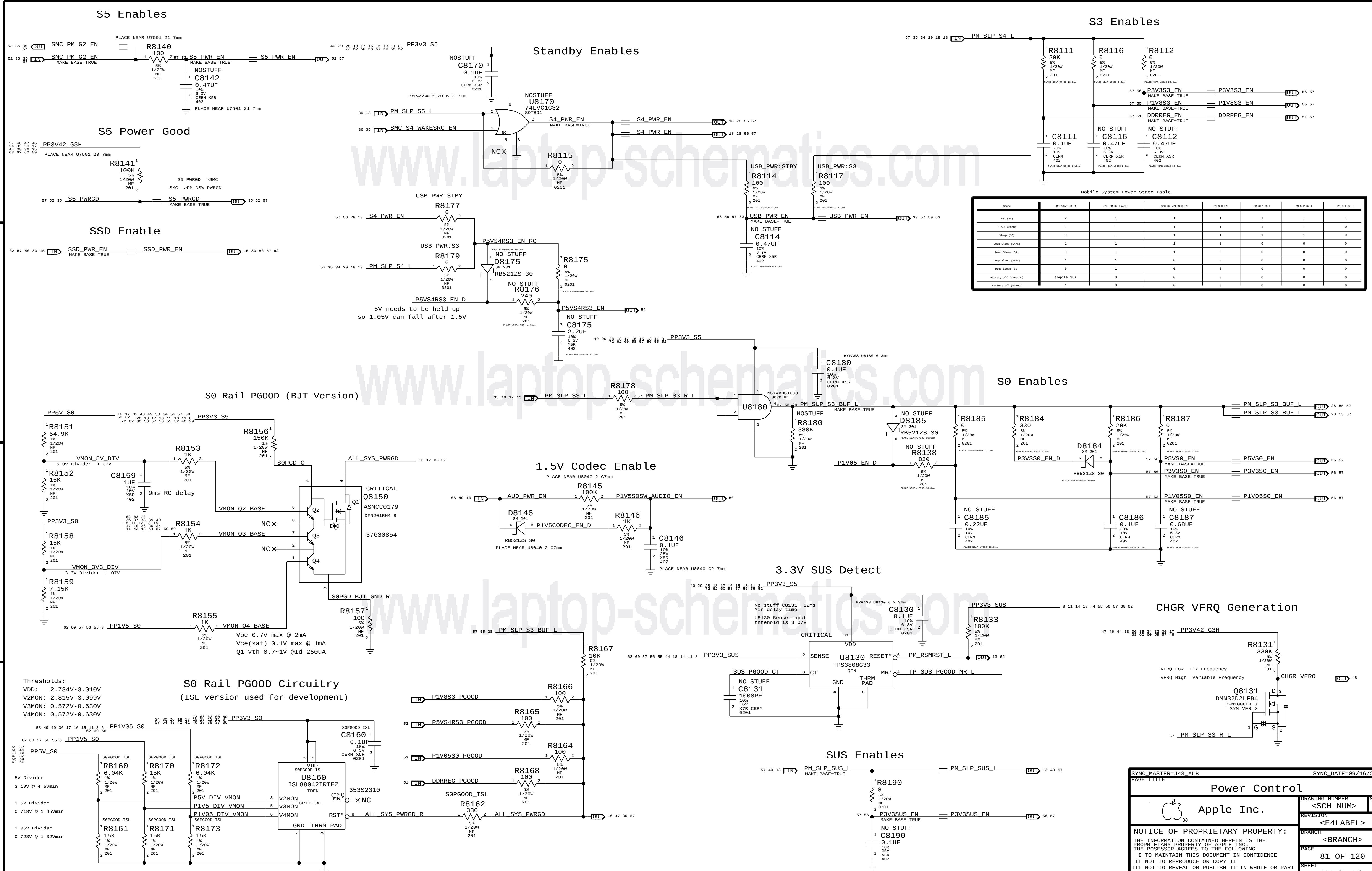

Mobile System Power State Table

State	SMC ADAPTER EN	SMC PM G2 ENABLE	SMC S4 WAKESRC EN	PM SUS EN	PM SLP S5 L	PM SLP S4 L	PM SLP S3 L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

SYNC_MASTER=J43_MLB SYNC_DATE=09/16/2012

PAGE TITLE: Power Control

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

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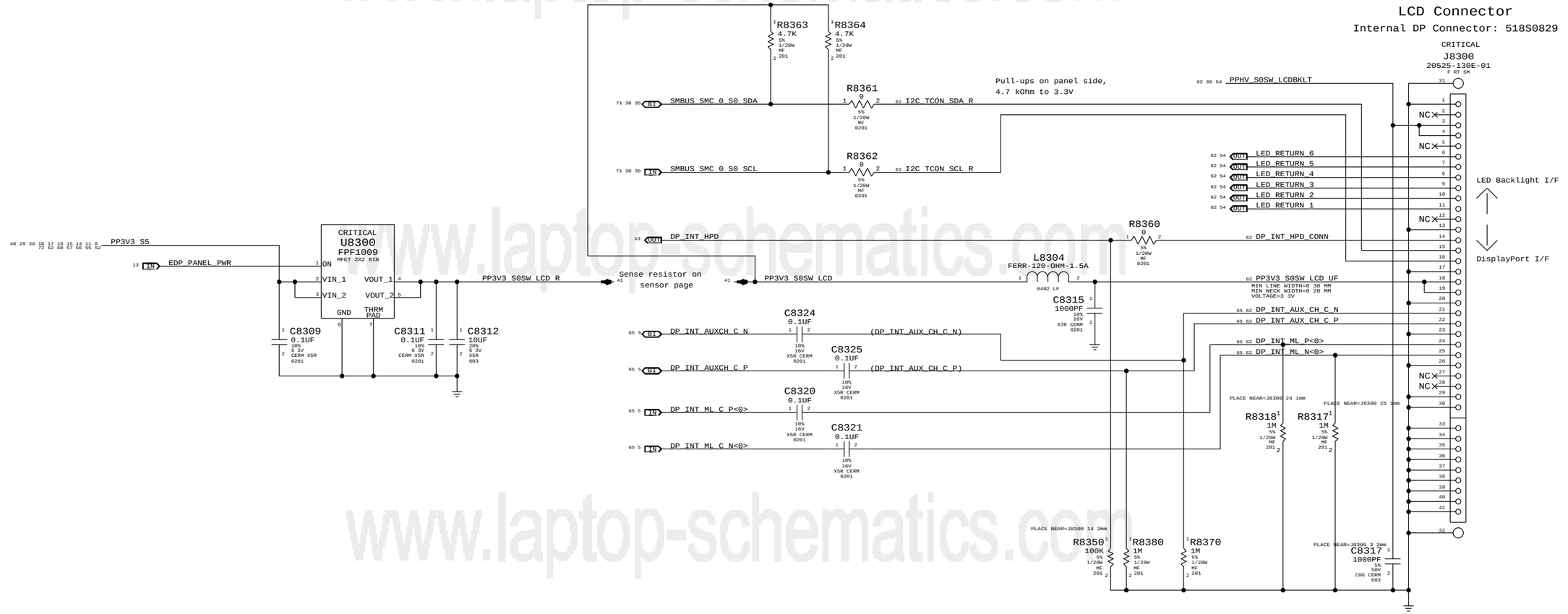

SYNC_MASTER=J43_MLB SYNC_DATE=09/11/2012

PAGE TITLE: Internal DisplayPort Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 83 OF 120
SHEET: 58 OF 73

LIO Connector

516S1036 (HIROSE 3.0mm RCPT)

CRITICAL

J9500
DF40CG3.0-48DS-0.4V

F ST SM

PP5V_S0
NOSTUFF
R9500 0 5% 1/20W MF 0201
VOLTAGE=5V
MIN LINE WIDTH=0 1MM
MIN NECK WIDTH=0 1MM

AUD_PWR_EN
PP5V_S0_ALT_AUD_LDO_EN
SPKRAMP_SHDN_L

PP1V5_S0SW_AUDIO
PP3V3_S0
C9520 0.1UF 10% 16V X5R CERM 0201
C9500 0.1UF 10% 16V X5R CERM 0201
BYPASS=J9500 1 5mm

SPKRAMP_INR_N
SPKRAMP_INR_P

GND VOID=TRUE

USB3_EXTB_D2R_N
USB3_EXTB_D2R_P
R9510 0 5% 1/20W MF 0201
NOSTUFF C9531 15PF 5% 25V NP0 CERM 0201
NOSTUFF C9532 15PF 5% 25V NP0 CERM 0201

USB3_EXTB_D2R_C_N
USB3_EXTB_D2R_C_P
R9520 0 5% 1/20W MF 0201
C9521 0.1UF 10% 16V X5R CERM 0201
C9522 0.1UF 10% 16V X5R CERM 0201

USB3_EXTB_D2R_RC_N
USB3_EXTB_D2R_RC_P

USB_EXTB_N
USB_EXTB_P

USB3_EXTB_R2D_N
USB3_EXTB_R2D_P

CRITICAL
D9511 ESD0P2RF-02LS TSSLP 2 1
D9510 ESD0P2RF-02LS TSSLP 2 1
D9520 ESD0P2RF-02LS TSSLP 2 1
D9521 ESD0P2RF-02LS TSSLP 2 1

PP3V42_G3H
C9510 0.1UF 10% 16V X5R CERM 0201
BYPASS=J9500 1 5mm

SMBUS_SMC_2_S3_SCL
SMBUS_SMC_2_S3_SDA
SYS_ONEWIRE
SMC_BC_ACOK
XDP_USB_EXTB_OC_L
USB_PWR_EN
FINSTACKSNS_ALERT_L
HDA_SYNC
HDA_RST_L
HDA_SDOUT
HDA_SDIN0
HDA_BIT_CLK

NOSTUFF C9550 10PF 5% 50V C0G CERM 0402

SYNC_MASTER=CLEAN_J41 SYNC_DATE=11/13/2012

PAGE TITLE: LIO Connector

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
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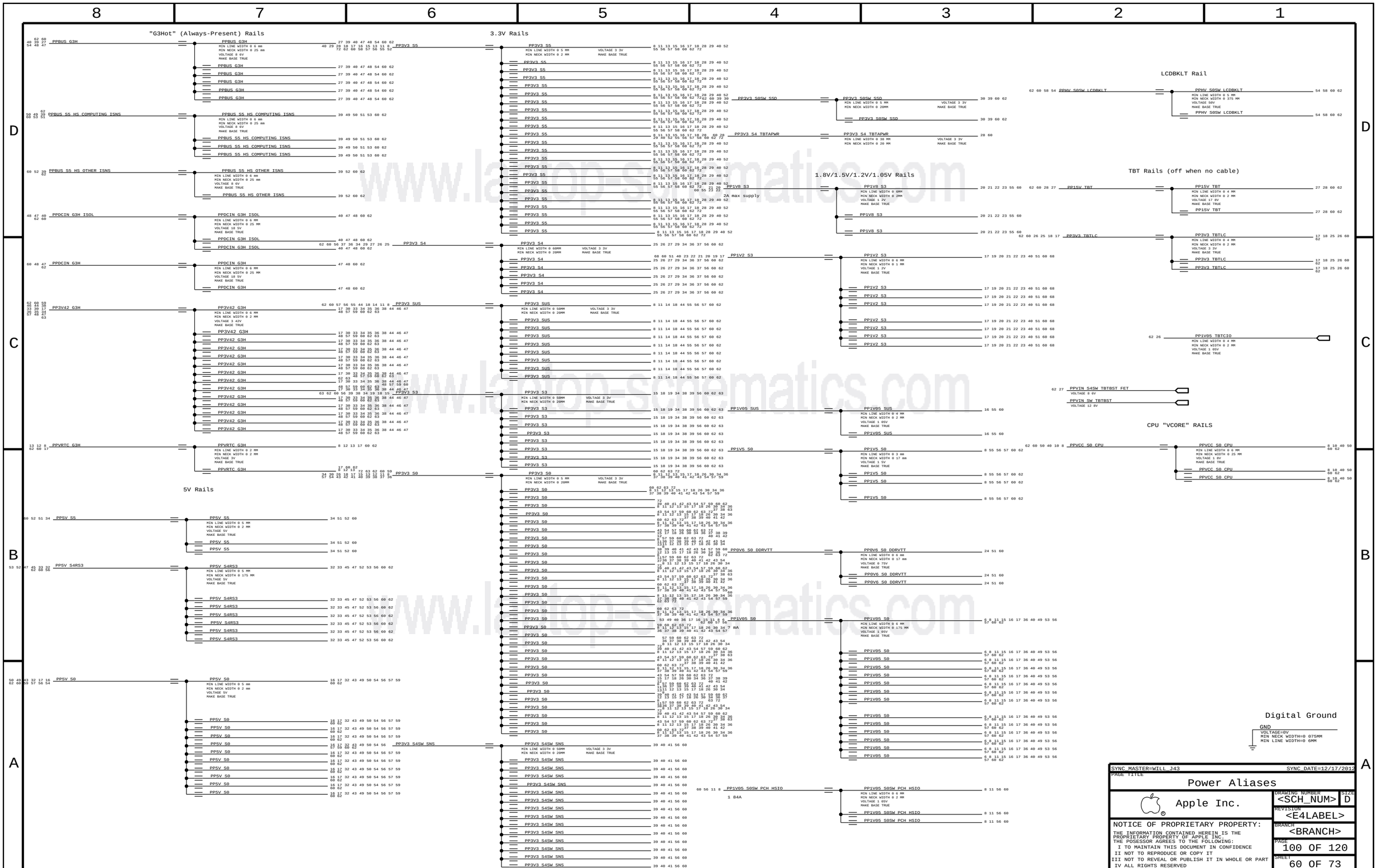
SHEET: 59 OF 73



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Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
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	BRANCH <BRANCH>
	PAGE 100 OF 120
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Memory Bit/Byte Swizzle

LPDDR3 Command/Address

	=MEM_A_A<5>	TRUE	MEM_A_CAA<0>		20 24 68
	=MEM_A_A<9>	TRUE	MEM_A_CAA<1>		20 24 68
	=MEM_A_A<6>	TRUE	MEM_A_CAA<2>		20 24 68
	=MEM_A_A<8>	TRUE	MEM_A_CAA<3>		20 24 68
	=MEM_A_A<7>	TRUE	MEM_A_CAA<4>		20 24 68
	=MEM_A_BA<2>	TRUE	MEM_A_CAA<5>		20 24 68
68 61 24 20 7	MEM_A_CAA<6>	TRUE	MEM_A_CAA<6>	7 20 24 61 68	
	=MEM_A_A<11>	TRUE	MEM_A_CAA<7>		20 24 68
	=MEM_A_A<15>	TRUE	MEM_A_CAA<8>		20 24 68
	=MEM_A_A<14>	TRUE	MEM_A_CAA<9>		20 24 68
	=MEM_A_A<13>	TRUE	MEM_A_CAB<0>		21 24 68
	=MEM_A_CAS_L	TRUE	MEM_A_CAB<1>		21 24 68
	=MEM_A_WE_L	TRUE	MEM_A_CAB<2>		21 24 68
	=MEM_A_RAS_L	TRUE	MEM_A_CAB<3>		21 24 68
	=MEM_A_BA<0>	TRUE	MEM_A_CAB<4>		21 24 68
	=MEM_A_A<2>	TRUE	MEM_A_CAB<5>		21 24 68
68 61 24 21 7	MEM_A_CAB<6>	TRUE	MEM_A_CAB<6>	7 21 24 61 68	
	=MEM_A_A<10>	TRUE	MEM_A_CAB<7>		21 24 68
	=MEM_A_A<1>	TRUE	MEM_A_CAB<8>		21 24 68
	=MEM_A_A<0>	TRUE	MEM_A_CAB<9>		21 24 68
68 61 24 21 20 7	MEM_A_ODT<0>	TRUE	MEM_A_ODT<0>	7 20 21 24 61 68	
61 7	TP_LPDDR3_RSVD1	TRUE	TP_LPDDR3_RSVD1	7 61	
61 7	TP_LPDDR3_RSVD2	TRUE	TP_LPDDR3_RSVD2	7 61	
	=MEM_B_A<5>	TRUE	MEM_B_CAA<0>		22 24 68
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	=MEM_B_A<7>	TRUE	MEM_B_CAA<4>		22 24 68
	=MEM_B_BA<2>	TRUE	MEM_B_CAA<5>		22 24 68
68 61 24 22 7	MEM_B_CAA<6>	TRUE	MEM_B_CAA<6>	7 22 24 61 68	
	=MEM_B_A<11>	TRUE	MEM_B_CAA<7>		22 24 68
	=MEM_B_A<15>	TRUE	MEM_B_CAA<8>		22 24 68
	=MEM_B_A<14>	TRUE	MEM_B_CAA<9>		22 24 68
	=MEM_B_A<13>	TRUE	MEM_B_CAB<0>		23 24 68
	=MEM_B_CAS_L	TRUE	MEM_B_CAB<1>		23 24 68
	=MEM_B_WE_L	TRUE	MEM_B_CAB<2>		23 24 68
	=MEM_B_RAS_L	TRUE	MEM_B_CAB<3>		23 24 68
	=MEM_B_BA<0>	TRUE	MEM_B_CAB<4>		23 24 68
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68 61 24 23 7	MEM_B_CAB<6>	TRUE	MEM_B_CAB<6>	7 23 24 61 68	
	=MEM_B_A<10>	TRUE	MEM_B_CAB<7>		23 24 68
	=MEM_B_A<1>	TRUE	MEM_B_CAB<8>		23 24 68
	=MEM_B_A<0>	TRUE	MEM_B_CAB<9>		23 24 68
68 61 24 23 22 7	MEM_B_ODT<0>	TRUE	MEM_B_ODT<0>	7 22 23 24 61 68	
61 7	TP_LPDDR3_RSVD3	TRUE	TP_LPDDR3_RSVD3	7 61	
61 7	TP_LPDDR3_RSVD4	TRUE	TP_LPDDR3_RSVD4	7 61	

MAKE BASE

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68 61 21 7	MEM_A_DQS_P<6>	TRUE	MEM_A_DQS_P<6>	7 21 61 68	
68 61 21 7	MEM_A_DQS_N<6>	TRUE	MEM_A_DQS_N<6>	7 21 61 68	
21	=MEM_A_DQS_P<7>	TRUE	MEM_A_DQS_P<7>	7 68	
21	=MEM_A_DQS_N<7>	TRUE	MEM_A_DQS_N<7>	7 68	

MAKE BASE

22	=MEM_B_DQ<0>	TRUE	MEM_B_DQ<12>	7 68	
22	=MEM_B_DQ<1>	TRUE	MEM_B_DQ<9>	7 68	
22	=MEM_B_DQ<2>	TRUE	MEM_B_DQ<10>	7 68	
22	=MEM_B_DQ<3>	TRUE	MEM_B_DQ<11>	7 68	
22	=MEM_B_DQ<4>	TRUE	MEM_B_DQ<13>	7 68	
22	=MEM_B_DQ<5>	TRUE	MEM_B_DQ<8>	7 68	
22	=MEM_B_DQ<6>	TRUE	MEM_B_DQ<14>	7 68	
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22	=MEM_B_DQ<8>	TRUE	MEM_B_DQ<0>	7 68	
22	=MEM_B_DQ<9>	TRUE	MEM_B_DQ<1>	7 68	
22	=MEM_B_DQ<10>	TRUE	MEM_B_DQ<2>	7 68	
22	=MEM_B_DQ<11>	TRUE	MEM_B_DQ<7>	7 68	
22	=MEM_B_DQ<12>	TRUE	MEM_B_DQ<4>	7 68	
22	=MEM_B_DQ<13>	TRUE	MEM_B_DQ<5>	7 68	
22	=MEM_B_DQ<14>	TRUE	MEM_B_DQ<6>	7 68	
22	=MEM_B_DQ<15>	TRUE	MEM_B_DQ<3>	7 68	
22	=MEM_B_DQ<16>	TRUE	MEM_B_DQ<28>	7 68	
22	=MEM_B_DQ<17>	TRUE	MEM_B_DQ<29>	7 68	
22	=MEM_B_DQ<18>	TRUE	MEM_B_DQ<30>	7 68	
22	=MEM_B_DQ<19>	TRUE	MEM_B_DQ<27>	7 68	
22	=MEM_B_DQ<20>	TRUE	MEM_B_DQ<24>	7 68	
22	=MEM_B_DQ<21>	TRUE	MEM_B_DQ<25>	7 68	
22	=MEM_B_DQ<22>	TRUE	MEM_B_DQ<31>	7 68	
22	=MEM_B_DQ<23>	TRUE	MEM_B_DQ<26>	7 68	
22	=MEM_B_DQ<24>	TRUE	MEM_B_DQ<20>	7 68	
22	=MEM_B_DQ<25>	TRUE	MEM_B_DQ<16>	7 68	
22	=MEM_B_DQ<26>	TRUE	MEM_B_DQ<23>	7 68	
22	=MEM_B_DQ<27>	TRUE	MEM_B_DQ<22>	7 68	
22	=MEM_B_DQ<28>	TRUE	MEM_B_DQ<21>	7 68	
22	=MEM_B_DQ<29>	TRUE	MEM_B_DQ<17>	7 68	
22	=MEM_B_DQ<30>	TRUE	MEM_B_DQ<18>	7 68	
22	=MEM_B_DQ<31>	TRUE	MEM_B_DQ<19>	7 68	
23	=MEM_B_DQ<32>	TRUE	MEM_B_DQ<44>	7 68	
23	=MEM_B_DQ<33>	TRUE	MEM_B_DQ<41>	7 68	
23	=MEM_B_DQ<34>	TRUE	MEM_B_DQ<42>	7 68	
23	=MEM_B_DQ<35>	TRUE	MEM_B_DQ<43>	7 68	
23	=MEM_B_DQ<36>	TRUE	MEM_B_DQ<45>	7 68	
23	=MEM_B_DQ<37>	TRUE	MEM_B_DQ<40>	7 68	
23	=MEM_B_DQ<38>	TRUE	MEM_B_DQ<46>	7 68	
23	=MEM_B_DQ<39>	TRUE	MEM_B_DQ<47>	7 68	
23	=MEM_B_DQ<40>	TRUE	MEM_B_DQ<32>	7 68	
68 61 23 7	MEM_B_DQ<33>	TRUE	MEM_B_DQ<33>	7 23 61 68	
23	=MEM_B_DQ<42>	TRUE	MEM_B_DQ<34>	7 68	
23	=MEM_B_DQ<43>	TRUE	MEM_B_DQ<39>	7 68	
23	=MEM_B_DQ<44>	TRUE	MEM_B_DQ<36>	7 68	
23	=MEM_B_DQ<45>	TRUE	MEM_B_DQ<37>	7 68	
23	=MEM_B_DQ<46>	TRUE	MEM_B_DQ<38>	7 68	
23	=MEM_B_DQ<47>	TRUE	MEM_B_DQ<35>	7 68	
23	=MEM_B_DQ<48>	TRUE	MEM_B_DQ<57>	7 68	
23	=MEM_B_DQ<49>	TRUE	MEM_B_DQ<56>	7 68	
23	=MEM_B_DQ<50>	TRUE	MEM_B_DQ<60>	7 68	
23	=MEM_B_DQ<51>	TRUE	MEM_B_DQ<59>	7 68	
23	=MEM_B_DQ<52>	TRUE	MEM_B_DQ<63>	7 68	
23	=MEM_B_DQ<53>	TRUE	MEM_B_DQ<62>	7 68	
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23	=MEM_B_DQ<55>	TRUE	MEM_B_DQ<61>	7 68	
23	=MEM_B_DQ<56>	TRUE	MEM_B_DQ<49>	7 68	
23	=MEM_B_DQ<57>	TRUE	MEM_B_DQ<51>	7 68	
23	=MEM_B_DQ<58>	TRUE	MEM_B_DQ<48>	7 68	
23	=MEM_B_DQ<59>	TRUE	MEM_B_DQ<53>	7 68	
23	=MEM_B_DQ<60>	TRUE	MEM_B_DQ<52>	7 68	
23	=MEM_B_DQ<61>	TRUE	MEM_B_DQ<55>	7 68	
23	=MEM_B_DQ<62>	TRUE	MEM_B_DQ<50>	7 68	
23	=MEM_B_DQ<63>	TRUE	MEM_B_DQ<54>	7 68	
22	=MEM_B_DQS_P<0>	TRUE	MEM_B_DQS_P<1>	7 68	
22	=MEM_B_DQS_N<0>	TRUE	MEM_B_DQS_N<1>	7 68	
22	=MEM_B_DQS_P<1>	TRUE	MEM_B_DQS_P<0>	7 68	
22	=MEM_B_DQS_N<1>	TRUE	MEM_B_DQS_N<0>	7 68	
22	=MEM_B_DQS_P<2>	TRUE	MEM_B_DQS_P<3>	7 68	
22	=MEM_B_DQS_N<2>	TRUE	MEM_B_DQS_N<3>	7 68	
22	=MEM_B_DQS_P<3>	TRUE	MEM_B_DQS_P<2>	7 68	
22	=MEM_B_DQS_N<3>	TRUE	MEM_B_DQS_N<2>	7 68	
23	=MEM_B_DQS_P<4>	TRUE	MEM_B_DQS_P<5>	7 68	
23	=MEM_B_DQS_N<4>	TRUE	MEM_B_DQS_N<5>	7 68	
23	=MEM_B_DQS_P<5>	TRUE	MEM_B_DQS_P<4>	7 68	
23	=MEM_B_DQS_N<5>	TRUE	MEM_B_DQS_N<4>	7 68	
23	=MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<7>	7 68	
23	=MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<7>	7 68	
68 61 23 7	MEM_B_DQS_P<6>	TRUE	MEM_B_DQS_P<6>	7 23 61 68	
68 61 23 7	MEM_B_DQS_N<6>	TRUE	MEM_B_DQS_N<6>	7 23 61 68	

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

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Functional Test Points

J3501: AirPort / BT Connector

FUNC TEST

TRUE	PP3V3_WLAN	(Need 6 TPs)	29 35 36 37 39
TRUE	WIFI_EVENT_L		29 35 36
TRUE	PCIE_AP_R2D_N		29 67
TRUE	PCIE_AP_R2D_P		29 67
TRUE	PCIE_CLK100M_AP_N		12 29 67
TRUE	PCIE_CLK100M_AP_P		12 29 67
TRUE	PCIE_AP_D2R_P		14 29 67
TRUE	PCIE_AP_D2R_N		14 29 67
TRUE	PCIE_WAKE_L		13 29 31
TRUE	AP_RESET_CONN_L		29
TRUE	AP_CLKREQ_O_L		29
TRUE	USB_BT_CONN_P		29 66
TRUE	USB_BT_CONN_N		29 66
TRUE	PP3V3_S4	(Need to add 8 GND TPs)	29 29 34 37 29 34 36 37 60 60 62

J3700: SSD Connector

FUNC TEST

TRUE	PP3V3_S0SW_SSD_FLT	(Need 5 TPs)	30
TRUE	PCIE_SSD_R2D_N<3..0>		30 65
TRUE	PCIE_SSD_R2D_P<3..0>		30 65
TRUE	PP3V3_S0		40 41 42 43 54 57 59 26 30 34 36 37 38 39 60 62 63 72 30
TRUE	SSD_RESET_CONN_L		30
TRUE	SSD_CLKREQ_CONN_L		30
TRUE	SMC_OOB1_R2D_CONN_L		30
TRUE	SMC_OOB1_D2R_CONN_L		30
TRUE	SSD_PCIE_SEL_L		30
TRUE	SSD_SR_EN_L		15 30
TRUE	SMC_PWRFAIL_WARN_L		30 35
TRUE	SSD_PWR_EN		15 30 56 57
TRUE	PCIE_SSD_D2R_N<3..0>		12 30 65
TRUE	PCIE_SSD_D2R_P<3..0>		12 30 65
TRUE	PCIE_CLK100M_SSD_N		12 30 65
TRUE	PCIE_CLK100M_SSD_P	(Need to add 6 GND TPs)	12 30 65

J4002: Camera Connector

FUNC TEST

TRUE	MIPI_CLK_CONN_N		32 70
TRUE	MIPI_CLK_CONN_P		32 70
TRUE	CAM_SENSOR_WAKE_L_CONN		32
TRUE	MIPI_DATA_CONN_N		32 70
TRUE	MIPI_DATA_CONN_P		32 70
TRUE	SMBUS_SMC_1_S0_SDA		14 32 35 38 41 42 67 71
TRUE	SMBUS_SMC_1_S0_SCL		14 32 35 38 41 42 67 71
TRUE	I2C_CAM_SCK		31 32
TRUE	I2C_CAM_SDA		31 32
TRUE	PP5V_S3RS0_ALSCAM_F	(Need TBD TPs) (Need to add TBD GND TPs)	32

J6100: LPC+SPI Connector

FUNC TEST

TRUE	SPI_ALT_IO3_HOLD_L		44
TRUE	SPI_ALT_IO2_WP_L		44
TRUE	LPC_AD<3..0>		14 35 67
TRUE	SPI_ALT_IO0_MOSI		44
TRUE	XDP_LPCPLUS_GPIO		15 16
TRUE	LPCPLUS_RESET_L		67
TRUE	SMC_TDO		35 36
TRUE	TP_SMC_TRST_L		
TRUE	TP_SMC_MD1		
TRUE	SMC_TX_L		35 36
TRUE	SPI_ALT_IO1_MISO		44
TRUE	LPC_FRAME_L		14 35 67
TRUE	SPIROM_USE_MLB		15 44
TRUE	PM_CLKRUN_L		13 35
TRUE	SPI_ALT_CLK		44
TRUE	SPI_ALT_CS_L		44
TRUE	LPC_SERIRQ		15 35
TRUE	LPC_PWRDWN_L		13 35
TRUE	SMC_TDI		35 36
TRUE	SMC_TCK		35 36 44
TRUE	SMC_RESET_L		35 36 44 48
TRUE	SMC_ROMBOOT		
TRUE	SMC_RX_L		35 36
TRUE	SMC_TMS	(Need to add 6 GND TPs)	35 36 44

J6000: Fan Connector

FUNC TEST

TRUE	PP5V_S0		16 17 32 43 49 50 54 56 57 59 60
TRUE	FAN_RT_TACH		43
TRUE	FAN_RT_PWM		43
		(Need to add 1 GND TP)	

J4800: IPD Flex Connector

FUNC TEST

TRUE	SMC_LID		34 35 36 46
TRUE	TPAD_SPI_MISO_R		34
TRUE	USB_TPAD_P		14 34 66
TRUE	USB_TPAD_N		14 34 66
TRUE	TPAD_SPI_CLK_R		34
TRUE	TPAD_WAKE_L		34
TRUE	TPAD_SPI_MOSI_R		34
TRUE	PP3V3_S4_IPD		34
TRUE	TPAD_SPI_CS_R_L		34
TRUE	TPAD_SPI_IF_EN_CONN		34
TRUE	TPAD_SPI_INT_S4_WAKE_L_CONN		34
TRUE	PP5V_S4_IPD		34
TRUE	TPAD_USB_IF_EN_CONN		34
TRUE	SMBUS_SMC_3_SDA		34 35 38 42 71
TRUE	SMBUS_SMC_3_SCL		34 35 38 42 71
TRUE	SMC_LSOC_RST_L		34 36
TRUE	PP3V42_G3H		17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	SMC_ONOFF_L	(Need to add 5 GND TPs)	34 35 36

J7000: DC-In Connector

FUNC TEST

TRUE	PPDCIN_G3H	(Need 4 TPs)	47 48 60 62
TRUE	PP5V_S4RS3	(Need 3 TPs)	32 33 45 47 52 53 56 60
		(Need to add 5 GND TPs)	

J6404: Speaker Connector

FUNC TEST

TRUE	SPKRAMP_ROUT_P		45 72
TRUE	SPKRAMP_ROUT_N		45 72
		(Need to add 3 GND TPs)	

J6950: Battery Connector

FUNC TEST

TRUE	PPVBAT_G3H_CONN	(Need 4 TPs)	46 48
TRUE	SMBUS_SMC_5_G3_SCL		35 38 46 48 71
TRUE	SMBUS_SMC_5_G3_SDA		35 38 46 48 71
TRUE	SYS_DETECT_L		46
		(Need to add 4 GND TPs near J7050 and 1 for shield)	

J8300: Internal DP Connector

FUNC TEST

TRUE	PPHV_S0SW_LCDBKLT	(Need 2 TPs)	54 58 60
TRUE	LED_RETURN_6		54 58
TRUE	LED_RETURN_5		54 58
TRUE	LED_RETURN_4		54 58
TRUE	LED_RETURN_3		54 58
TRUE	LED_RETURN_2		54 58
TRUE	LED_RETURN_1		54 58
TRUE	DP_INT_HPD_CONN		58
TRUE	I2C_TCON_SDA_R		58
TRUE	I2C_TCON_SCL_R		58
TRUE	PP3V3_S0SW_LCD_UF	(Need 2 TPs)	58
TRUE	DP_INT_AUX_CH_C_N		58 65
TRUE	DP_INT_AUX_CH_C_P		58 65
TRUE	DP_INT_ML_P<0>		58 65
TRUE	DP_INT_ML_N<0>		58 65
		(Need to add 5 GND TPs)	

J7715: KB BKLT Connector

FUNC TEST

TRUE	KBDLED_ANODE		54
TRUE	KBDLED_FB		54
		(Need to add 2 GND TPs)	

J1800: XDP Connector

(Only a subset are needed for FCT HVM test fixture)

FUNC TEST

J726	TRUE	XDP_CPU_TCK	6 16 65
J777	TRUE	XDP_PCH_TCK	12 16 67
J778	TRUE	XDP_CPU_TDI	6 16 65
J779	TRUE	XDP_CPU_TDO	6 16 65
J780	TRUE	XDP_CPUPCH_TRST_L	6 12 16 65
J781	TRUE	XDP_CPU_TMS	6 16 65
J782	TRUE	XDP_PCH_TMS	12 16 67
J783	TRUE	XDP_PCH_TDI	12 16 67
J784	TRUE	XDP_PCH_TDO	12 16 67
J785	TRUE	XDP_CPU_PREQ_L	6 16 65
J786	TRUE	XDP_CPU_PRDY_L	6 16 65
J787	TRUE	XDP_CPU_VCCST_PWRGD	16
J788	TRUE	PM_RSMRST_L	13 57
J789	TRUE	XDP_SYS_PWROK	16
J790	TRUE	PM_SYSRST_L	13 17 35
J791	TRUE	CPU_CFG<3>	6 16 65
J792	TRUE	PP1V05_S0	6 8 11 15 16 17 36 40 49 53 56 57 60 62
		(Need to add 2 GND TPs)	

J793 TRUE GND

Misc Voltages & Control Signals

FUNC TEST

TRUE	PPBUS_G3H	27 39 40 47 48 54 60
TRUE	PPVIN_S4SW_TBTBST_FET	27 60
TRUE	PPBUS_S5_HS_COMPUTING_ISNS	39 49 50 51 53 60
TRUE	PPDCIN_G3H	47 48 60 62
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	PPVRTC_G3H	8 12 13 17 60
TRUE	PP3V3_S5	8 11 13 15 16 17 18 28 29 40 52 55 56 57 58 60 72
TRUE	PP3V3_SUS	8 11 14 18 44 55 56 57 60
TRUE	PP3V3_S3	15 18 19 34 38 39 56 60 63
TRUE	PP3V3_S0	60 62 63 72
TRUE	PP3V3_S0SW_SSD	8 12 13 15 16 17 18 26 30 34 36 37 38 39 40 41 42 43 54 57 59
TRUE	PP1V5_S0	30 39 60
TRUE	PP1V05_S0	8 55 56 57 60
TRUE	PP15V_TBT	6 8 13 15 16 17 36 40 49 53 56 57 60 62
TRUE	PP3V3_TBTLC	27 28 60
TRUE	PP1V05_TBT	17 18 25 26 60
TRUE	PPVCC_S0_CPU	26
TRUE	PP1V05_TBTCIO	8 10 40 50 60
TRUE	PPBUS_S5_HS_OTHER_ISNS	26 60
TRUE	PPDCIN_G3H_ISOL	39 52 60
TRUE	PP3V3_S4	40 47 48 60
		(Need to add 27 GND TPs)

NO_TEST Nets

NO TEST | MAKE BASE

62	NC_PCIE_CLK100M_SDP	TRUE	TRUE	NC_PCIE_CLK100M_SDP	62	
62	NC_PCIE_CLK100M_SDN	TRUE	TRUE	NC_PCIE_CLK100M_SDN	62	
62 12	NC_PCIE_CLK100M_FWP	TRUE	TRUE	NC_PCIE_CLK100M_FWP	12 62	
62 12	NC_PCIE_CLK100M_FWN	TRUE	TRUE	NC_PCIE_CLK100M_FWN	12 62	
62 14	NC_PCIE_FW_D2RP	TRUE	TRUE	NC_PCIE_FW_D2RP	14 62	
62 14	NC_PCIE_FW_D2RN	TRUE	TRUE	NC_PCIE_FW_D2RN	14 62	
62 14	NC_PCIE_FW_R2D_CP	TRUE	TRUE	NC_PCIE_FW_R2D_CP	14 62	
62 14	NC_PCIE_FW_R2D_CN	TRUE	TRUE	NC_PCIE_FW_R2D_CN	14 62	
62 14	NC_USB_IRP	TRUE	TRUE	NC_USB_IRP	14 62	
62 14	NC_USB_IRN	TRUE	TRUE	NC_USB_IRN	14 62	
62 14	NC_USB_CAMERAP	TRUE	TRUE	NC_USB_CAMERAP	14 62	
62 14	NC_USB_CAMERAN	TRUE	TRUE	NC_USB_CAMERAN	14 62	
62 14	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP	14 62	
62 14	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN	14 62	
65	DP_INT_ML_C_P<3..1>	TRUE	TRUE	NC_INT_ML_CP<3..1>	5	
65	DP_INT_ML_C_N<3..1>	TRUE	TRUE	NC_INT_ML_CN<3..1>	5	
62 12	NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1	12 62	
62 13	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L	13 62	
62 14	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK	14 62	
62 14	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA	14 62	
62 14	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L	14 62	
62 35	NC_SMC_SYS_LED	TRUE	TRUE	NC_SMC_SYS_LED	35 62	
62	NC_IR_RX_OUT_RC	TRUE	TRUE	NC_IR_RX_OUT_RC	62	
62	NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP	62	
62	NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN	62	
62 35	NC_SMC_GFX_OVERTEMP	TRUE	TRUE	NC_SMC_GFX_OVERTEMP	35 62	
62 35	NC_SMC_GFX_THROTTLE_L	TRUE	TRUE	NC_SMC_GFX_THROTTLE_L	35 62	
62 35	NC_SMC_FAN_1_CTL	TRUE	TRUE	NC_SMC_FAN_1_CTL	35 62	
62 35	NC_SMC_FAN_1_TACH	TRUE	TRUE	NC_SMC_FAN_1_TACH	35 62	
62 35	NC_SMC_FAN_5_CTL	TRUE	TRUE	NC_SMC_FAN_5_CTL	35 62	
62	NC_ENET_ASF_GPIO	TRUE	TRUE	NC_ENET_ASF_GPIO	62	
62	NC_SMC_MPM5_LED_PWR	TRUE	TRUE	NC_SMC_MPM5_LED_PWR	62	
62	NC_SMC_MPM5_LED_CHG	TRUE	TRUE	NC_SMC_MPM5_LED_CHG	62	
62 35	NC_SMC_T25_EN_L	TRUE	TRUE	NC_SMC_T25_EN_L	35 62	
62 35	NC_SMC_DP_HPD_L	TRUE	TRUE	NC_SMC_DP_HPD_L	35 62	
62 35	NC_SMBUS_SMC_4_ASF_SCL	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SCL	35 62	
62 35	NC_SMBUS_SMC_4_ASF_SDA	TRUE	TRUE	NC_SMBUS_SMC_4_ASF_SDA	35 62	
62 35	NC_BDV_BKL_PWM	TRUE	TRUE	NC_BDV_BKL_PWM	35 62	
69	TBT_B_R2D_C_P<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CP<1..0>	25	
69	TBT_B_R2D_C_N<1..0>	TRUE	TRUE	NC_TBT_B_R2D_CN<1..0>	25	
69	TBT_B_D2R_P<1..0>	TRUE	TRUE	NC_TBT_B_D2RP<1..0>	25	
69	TBT_B_D2R_N<1..0>	TRUE	TRUE	NC_TBT_B_D2RN<1..0>	25	
62 25	NC_TBT_B_LSTX	TRUE	TRUE	NC_TBT_B_LSTX	25 62	
69 62	NC_DP_TBTPB_ML_CP<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CP<3..1:2>	62 69	
69 62	NC_DP_TBTPB_ML_CN<3..1:2>	TRUE	TRUE	NC_DP_TBTPB_ML_CN<3..1:2>	62 69	
69 62 25	NC_DP_TBTPB_AUXCH_CP	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CP	25 62 69	
69 62 25	NC_DP_TBTPB_AUXCH_CN	TRUE	TRUE	NC_DP_TBTPB_AUXCH_CN	25 62 69	
25	TP_DP_TBTSRC_ML_CP<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3>		
25	TP_DP_TBTSRC_ML_CN<3>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3>		
25	TP_DP_TBTSRC_ML_CP<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<2>		
25	TP_DP_TBTSRC_ML_CN<2>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<2>		
62 25	NC_DP_TBTSRC_ML_CP<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<1>	25 62	
62 25	NC_DP_TBTSRC_ML_CN<1>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<1>	25 62	
25	TP_DP_TBTSRC_ML_CP<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<0>		
25	TP_DP_TBTSRC_ML_CN<0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<0>		
62 25	NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP	25 62	
62 25	NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN	25 62	

CPU/PCH

SMC

TBT

Unused nets with offpage

(Nets with offpages not used on this project)

PCH_BT_UART_D2R	15
PCH_BT_UART_R2D	15
PCH_BT_UART_RTS_L	15
PCH_BT_UART_CTS_L	15
AUD_SPI_CS_L	15
AUD_SPI_CLK	15
AUD_SPI_MISO	15
AUD_SPI_MOSI	15
HDMITBTMUX_LATCH	13
HDD_PWR_EN	15
WOL_EN	14
BT_PWRRST_L	15
HDMITBTMUX_FLAG	13
FW_PWR_EN	
FW_PME_L	
ENET_MEDIA_SENSE	15
LCD_PSR_EN	15
LCD_IRQ_L	15
ODD_PWR_EN_L	13
ENET_LOW_PWR	13
AUD_IP_PERIPHERAL_DET	
AUD_I2C_INT_L	
AP_PCIE_DEV_WAKE	13

SYNC_MASTER=WILL_J43 SYNC_DATE=12/17/2012

PAGE TITLE: Func Test / No Test

Apple Inc.

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REVISION: <E4LABEL>

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Functional Test Points

J9500: LIO Connector

FUNC TEST		
TRUE	AUD_PWR_EN	13 57 59
TRUE	PP5V_S0_ALT_AUD_LDO_EN	59
TRUE	SPKRAMP_SHDN_L	45 59
TRUE	PP1V5_S0SW_AUDIO	56 59
TRUE	PP3V3_S0	60 62 72 5 11 12 13 15 17 18 26 30 34 36 37 38 39 40 41 42 43 54 57 59
TRUE	SPKRAMP_INR_N	45 59 72
TRUE	SPKRAMP_INR_P	45 59 72
TRUE	USB3_EXTB_D2R_RC_N	59 63 66
TRUE	USB3_EXTB_D2R_RC_P	59 63 66
TRUE	USB_EXTB_N	14 59 66
TRUE	USB_EXTB_P	14 59 66
TRUE	USB3_EXTB_R2D_N	59 63 66
TRUE	USB3_EXTB_R2D_P	59 63 66
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63
TRUE	SMBUS_SMC_2_S3_SCL	35 38 59 71
TRUE	SMBUS_SMC_2_S3_SDA	35 38 59 71
TRUE	SYS_ONEWIRE	35 59
TRUE	SMC_BC_ACOK	35 36 48 59
TRUE	XDP_USB_EXTB_OC_L	14 16 59
TRUE	USB_PWR_EN	33 57 59
TRUE	FINSTACKSNS_ALERT_L	37 59
TRUE	HDA_SYNC	12 59 67
TRUE	HDA_RST_L	12 59 67
TRUE	HDA_SDOUT	12 59 67
TRUE	HDA_SDIN0	12 59 67
TRUE	HDA_BIT_CLK (Need to add 5 GND TPs)	12 59 67

J6955: HALL EFFECT Connector

FUNC TEST		
TRUE	SMC_LID_R	46
TRUE	PP3V42_G3H	17 30 33 34 35 36 38 44 46 47 48 57 59 60 62 63

Power Aliases

63 62 60 56 39 38 34 19 18 15 PP3V3_S3 = PP3V3_S3 15 18 19 34 38 39 56 60 62 63

NO_TEST Nets

		NO TEST	MAKE BASE		
66 63 14	NC_USB3RPCIE_SD_D2RP	TRUE	TRUE	NC_USB3RPCIE_SD_D2RP	14 63 66
66 63 14	NC_USB3RPCIE_SD_D2RN	TRUE	TRUE	NC_USB3RPCIE_SD_D2RN	14 63 66
66 63 14	NC_USB3RPCIE_SD_R2D_CP	TRUE	TRUE	NC_USB3RPCIE_SD_R2D_CP	14 63 66 CPU/PCH
66 63 14	NC_USB3RPCIE_SD_R2D_CN	TRUE	TRUE	NC_USB3RPCIE_SD_R2D_CN	14 63 66
63 37 35	NC_SMC_ADC16	TRUE	TRUE	NC_SMC_ADC16	35 37 63 SMC

Bead Probes

66 59 14	USB3_EXTB_D2R_N	SM	BEAD-PROBE	BPA511
66 59 14	USB3_EXTB_D2R_P	SM	BEAD-PROBE	BPA510
66 63 59	USB3_EXTB_D2R_RC_N	SM	BEAD-PROBE	BPA520
66 63 59	USB3_EXTB_D2R_RC_P	SM	BEAD-PROBE	BPA521
66 59 14	USB3_EXTB_R2D_C_N	SM	BEAD-PROBE	BPA513
66 59 14	USB3_EXTB_R2D_C_P	SM	BEAD-PROBE	BPA512
66 63 59	USB3_EXTB_R2D_N	SM	BEAD-PROBE	BPA523
66 63 59	USB3_EXTB_R2D_P	SM	BEAD-PROBE	BPA522

Unused nets with offpage

(Nets with offpages not used on this project)

SD_RESET_L	15
XDP_SDCONN_STATE_CHANGE_L	15 16
SD_PWR_EN	15

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE: Project FCT/NC/Aliases

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J41/J43 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP ISL2 ISL3 ISL4 ISL5 ISL6 ISL7 ISL8 ISL9 ISL10 ISL11 BOTTOM	NO TYPE BGA MEM TERM	MM	16 2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP BOTTOM	Y	=50 OHM SE	=50 OHM SE			
DEFAULT	ISL2 ISL11	Y	=45 OHM SE	=45 OHM SE			
DEFAULT	ISL3 ISL10	Y	=45 OHM SE	=45 OHM SE			
DEFAULT	ISL4 ISL9	Y	=45 OHM SE	=45 OHM SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4 OHM SE	TOP BOTTOM	Y	0 310 MM	0 310 MM			
27P4 OHM SE	ISL2 ISL11	Y	0 182 MM	0 182 MM			
27P4 OHM SE	ISL3 ISL10	Y	0 182 MM	0 182 MM			
27P4 OHM SE	ISL4 ISL9	Y	0 182 MM	0 182 MM			
27P4 OHM SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35 OHM SE	TOP BOTTOM	Y	0 195 MM	0 195 MM			
35 OHM SE	ISL2 ISL11	Y	0 125 MM	0 125 MM			
35 OHM SE	ISL3 ISL10	Y	0 125 MM	0 125 MM			
35 OHM SE	ISL4 ISL9	Y	0 125 MM	0 125 MM			
35 OHM SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40 OHM SE	TOP BOTTOM	Y	0 170 MM	0 170 MM			
40 OHM SE	ISL2 ISL11	Y	0 096 MM	0 096 MM			
40 OHM SE	ISL3 ISL10	Y	0 096 MM	0 096 MM			
40 OHM SE	ISL4 ISL9	Y	0 099 MM	0 099 MM			
40 OHM SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45 OHM SE	TOP BOTTOM	Y	0 135 MM	0 135 MM			
45 OHM SE	ISL2 ISL11	Y	0 075 MM	0 075 MM			
45 OHM SE	ISL3 ISL10	Y	0 075 MM	0 075 MM			
45 OHM SE	ISL4 ISL9	Y	0 080 MM	0 080 MM			
45 OHM SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50 OHM SE	TOP BOTTOM	Y	0 110 MM	0 110 MM			
50 OHM SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55 OHM SE	TOP BOTTOM	Y	0 090 MM	0 090 MM			
55 OHM SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70 OHM DIFF	TOP BOTTOM	Y	0 165 MM	0 165 MM		0 110 MM	0 110 MM
70 OHM DIFF	ISL2 ISL11	Y	0 105 MM	0 105 MM		0 100 MM	0 100 MM
70 OHM DIFF	ISL3 ISL10	Y	0 105 MM	0 105 MM		0 100 MM	0 100 MM
70 OHM DIFF	ISL4 ISL9	Y	0 110 MM	0 110MM		0 095 MM	0 095 MM
70 OHM DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80 OHM DIFF	TOP BOTTOM	Y	0 132 MM	0 132 MM		0 130 MM	0 130 MM
80 OHM DIFF	ISL2 ISL11	Y	0 081 MM	0 081 MM		0 115 MM	0 115 MM
80 OHM DIFF	ISL3 ISL10	Y	0 081 MM	0 081 MM		0 115 MM	0 115 MM
80 OHM DIFF	ISL4 ISL9	Y	0 088 MM	0 088 MM		0 110 MM	0 110 MM
80 OHM DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90 OHM DIFF	TOP BOTTOM	Y	0 115 MM	0 115 MM		0 200 MM	0 200 MM
90 OHM DIFF	ISL2 ISL11	Y	0 070 MM	0 070 MM		0 180 MM	0 180 MM
90 OHM DIFF	ISL3 ISL10	Y	0 070 MM	0 070 MM		0 180 MM	0 180 MM
90 OHM DIFF	ISL4 ISL9	Y	0 076 MM	0 076 MM		0 180 MM	0 180 MM
90 OHM DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1 1 SPACING	*	0 100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x DIELECTRIC	TOP BOTTOM	0 071 MM	?
1x DIELECTRIC	ISL3 ISL10	0 053 MM	?
1x DIELECTRIC	ISL4 ISL9	0 050 MM	?
1x DIELECTRIC	*	0 090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P075MM	*	0.075 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P075MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	P070MM_BGA

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P070MM_BGA	*			0.070 MM	5 MM		0.075 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73 OHM DIFF	TOP BOTTOM	Y	0 165 MM	0 165 MM		0 150 MM	0 150 MM
73 OHM DIFF	ISL2 ISL11	Y	0 106 MM	0 106 MM		0 150 MM	0 150 MM
73 OHM DIFF	ISL3 ISL10	Y	0 106 MM	0 106 MM		0 150 MM	0 150 MM
73 OHM DIFF	ISL4 ISL9	Y	0 110 MM	0 110 MM		0 150 MM	0 150 MM
73 OHM DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85 OHM DIFF	TOP BOTTOM	Y	0 120 MM	0 120 MM		0 150 MM	0 150 MM
85 OHM DIFF	ISL2 ISL11	Y	0 078 MM	0 078 MM		0 160 MM	0 160 MM
85 OHM DIFF	ISL3 ISL10	Y	0 078 MM	0 078 MM		0 160 MM	0 160 MM
85 OHM DIFF	ISL4 ISL9	Y	0 082 MM	0 082 MM		0 140 MM	0 140 MM
85 OHM DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

SYNC MASTER=J43_MLB SYNC DATE=10/24/2012

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PCB Rule Definitions

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD
CPU 27P4S	*	27P4 OHM SE	=27P4 OHM SE	=27P4 OHM SE	=27P4 OHM SE	0 100 MM	0 100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU AGTL	TOP BOTTOM	=2x DIELECTRIC	?
CPU AGTL	*	=STANDARD	?

Note CPU 8MIL and CPU ITP can be converted back to TABLE SPACING RULE once rdar //10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU 8MIL	*	*	CPU 8MIL 2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU 8MIL 2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU ITP	*	*	CPU ITP 2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU ITP 2ANY	*	=4x DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU COMP	CPU COMP	*	CPU COMP 2SELF
CPU COMP	*	*	CPU COMP 2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU COMP 2SELF	TOP BOTTOM	=6x DIELECTRIC	?
CPU COMP 2OTHER	TOP BOTTOM	=10x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU COMP 2SELF	*	=4x DIELECTRIC	?
CPU COMP 2OTHER	*	=6x DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU VCCSENSE	CPU VCCSENSE	*	CPU VCCSENSE 2SELF
CPU VCCSENSE	*	*	CPU VCCSENSE 2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU VCCSENSE 2SELF	TOP BOTTOM	=6x DIELECTRIC	?
CPU VCCSENSE 2OTHER	TOP BOTTOM	=10x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU VCCSENSE 2SELF	*	=4x DIELECTRIC	?
CPU VCCSENSE 2OTHER	*	=6x DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE 80D	*	80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF
CLK PCIE 80D	*	80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK PCIE	CLK PCIE	*	CLK PCIE 2SELF
CLK PCIE	*	*	CLK PCIE 2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK PCIE 2SELF	TOP BOTTOM	=6x DIELECTRIC	?
CLK PCIE 2OTHER	TOP BOTTOM	=10x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK PCIE 2SELF	*	=4x DIELECTRIC	?
CLK PCIE 2OTHER	*	=6x DIELECTRIC	?

CPU PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE CPU TX	PCIE CPU TX	*	PCIE TX2TX
PCIE CPU RX	PCIE CPU RX	*	PCIE RX2RX
PCIE CPU TX	* CPU TX	*	PCIE TX2OTHERTX
PCIE CPU RX	* CPU RX	*	PCIE RX2OTHERRX
PCIE CPU TX	* CPU RX	*	PCIE TX2RX
PCIE CPU RX	* CPU TX	*	PCIE RX2TX
PCIE CPU TX	* TX	*	PCIE 2OTHERHS
PCIE CPU RX	* TX	*	PCIE 2OTHERHS
PCIE CPU TX	* RX	*	PCIE 2OTHERHS
PCIE CPU RX	* RX	*	PCIE 2OTHERHS
PCIE CPU TX	*	*	PCIE 2OTHER
PCIE CPU RX	*	*	PCIE 2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE TX2TX	TOP BOTTOM	=5x DIELECTRIC	?
PCIE RX2RX	TOP BOTTOM	=5x DIELECTRIC	?
PCIE TX2OTHERTX	TOP BOTTOM	=5x DIELECTRIC	?
PCIE RX2OTHERRX	TOP BOTTOM	=5x DIELECTRIC	?
PCIE TX2RX	TOP BOTTOM	=7x DIELECTRIC	?
PCIE RX2TX	TOP BOTTOM	=7x DIELECTRIC	?
PCIE 2OTHERHS	TOP BOTTOM	=6x DIELECTRIC	?
PCIE 2OTHER	TOP BOTTOM	=5x DIELECTRIC	?

PCH PCIE Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE PCH TX	PCIE PCH TX	*	PCIE TX2TX
PCIE PCH RX	PCIE PCH RX	*	PCIE RX2RX
PCIE PCH TX	* PCH TX	*	PCIE TX2OTHERTX
PCIE PCH RX	* PCH RX	*	PCIE RX2OTHERRX
PCIE PCH TX	* PCH RX	*	PCIE TX2RX
PCIE PCH RX	* PCH TX	*	PCIE RX2TX
PCIE PCH TX	* TX	*	PCIE 2OTHERHS
PCIE PCH RX	* TX	*	PCIE 2OTHERHS
PCIE PCH TX	* RX	*	PCIE 2OTHERHS
PCIE PCH RX	* RX	*	PCIE 2OTHERHS
PCIE PCH TX	*	*	PCIE 2OTHER
PCIE PCH RX	*	*	PCIE 2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE TX2TX	*	=2 5x DIELECTRIC	?
PCIE RX2RX	*	=2 5x DIELECTRIC	?
PCIE TX2OTHERTX	*	=4x DIELECTRIC	?
PCIE RX2OTHERRX	*	=4x DIELECTRIC	?
PCIE TX2RX	*	=6x DIELECTRIC	?
PCIE RX2TX	*	=6x DIELECTRIC	?
PCIE 2OTHERHS	*	=4x DIELECTRIC	?
PCIE 2OTHER	*	=3x DIELECTRIC	?

SOURCE 471984 Chief River MS PDG 1 0 and the spacing rule is adjusted per SI team feedback

Note: DisplayPort tables are on Page 113

CPU Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
CPU PECI	CPU 45S	CPU COMP	CPU_PECI	6 36
PM_SYNC	CPU 45S	CPU AGTL	PM_SYNC	
PM_MEM_PWRGD	CPU 45S	CPU AGTL	PM_MEM_PWRGD	
	CPU 45S	CPU ITP	XDP_DBRESET_L	16 17
	CPU 45S	CPU ITP	XDP_CPU_PRDY_L	6 16 62
	CPU 45S	CPU ITP	XDP_CPU_PREQ_L	6 16 62
	CPU 27P4S	CPU COMP	EDP_COMP	
	CPU 27P4S	CPU COMP	CPU_PEG_COMP	
CPU_SM_RCOMP	CPU 27P4S	CPU COMP	CPU_SM_RCOMP<0>	6
CPU_SM_RCOMP	CPU 27P4S	CPU COMP	CPU_SM_RCOMP<1>	6
CPU_SM_RCOMP	CPU 27P4S	CPU COMP	CPU_SM_RCOMP<2>	6
	CPU 45S	CPU ITP	CPU_CFG<11..0>	6 16 62
CPU_CATERR_L	CPU 45S	CPU AGTL	CPU_CATERR_L	6 35
	CPU 45S	CPU AGTL	CPU_VCCIO_SEL	
CPU_PROCHOT_L	CPU 45S	CPU AGTL	CPU_PROCHOT_L	6 35 36 49
CPU_PWRGD	CPU 45S	CPU AGTL	CPU_PWRGD	6
PM_THRMTRIP_L	CPU 45S	CPU RMTL	PM_THRMTRIP_L	15 36
DMI_CLK100M	CLK PCIE 80D	CLK PCIE	DMI_CLK100M_CPU_P	
DMI_CLK100M	CLK PCIE 80D	CLK PCIE	DMI_CLK100M_CPU_N	
DPLL_REF_CLK120M	CLK PCIE 80D	CLK PCIE	DPLL_REF_CLKP	
DPLL_REF_CLK120M	CLK PCIE 80D	CLK PCIE	DPLL_REF_CLKN	
ITPCPU_CLK100M	CLK PCIE 80D	CLK PCIE	ITPCPU_CLK100M_P	
ITPCPU_CLK100M	CLK PCIE 80D	CLK PCIE	ITPCPU_CLK100M_N	
ITPCPU_CLK100M	CLK PCIE 80D	CLK PCIE	ITPXDP_CLK100M_P	
ITPCPU_CLK100M	CLK PCIE 80D	CLK PCIE	ITPXDP_CLK100M_N	
ITPCPU_CLK100M	CLK PCIE 80D	CLK PCIE	XDP_CPU_CLK100M_P	
ITPCPU_CLK100M	CLK PCIE 80D	CLK PCIE	XDP_CPU_CLK100M_N	
XDP_TDI	CPU 45S	CPU ITP	XDP_CPU_TDI	6 16 62
XDP_TDO	CPU 45S	CPU ITP	XDP_CPU_TDO	6 16 62
XDP_TMS	CPU 45S	CPU ITP	XDP_CPU_TMS	6 16 62
XDP_TCK	CPU 45S	CPU ITP	XDP_CPU_TCK	6 16 62
XDP_TRST_L	CPU 45S	CPU ITP	XDP_CPUPCH_TRST_L	6 12 16 62
XDP_BPM_L	CPU 45S	CPU ITP	XDP_BPM_L<1..0>	6 16
	CPU 45S	CPU ITP	XDP_BPM_L<7..2>	6 16
	CPU 45S	CPU ITP	XDP_OBSDATA_B<3..0>	
	CPU 45S	CPU ITP	CPU_CFG<15..12>	6 16
(ESB_CPURST_L)	CPU 45S	CPU ITP	XDP_CPURST_L	16
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 49
CPU_VCCSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 49
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
CPU_VCCIOSENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
CPU_AXG_SENSE	SENSE_1TO1_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L	8 49
CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU_VIDSCLK	8 49
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT	8 49
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<3..0>	12 30
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<3..0>	12 30
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<3..0>	30 62
	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<3..0>	30 62
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<3..0>	
	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<3..0>	
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<3..0>	12 30 62
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<3..0>	12 30 62
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P	12 30 62
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N	12 30 62
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK0_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_P<3..0>	5 25
	DP_80D	DP_TX	DP_TBTSNK0_ML_C_N<3..0>	5 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_P	13 25
	DP_80D	DP_AUX	DP_TBTSNK0_AUXCH_C_N	13 25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_P<3..0>	25
DP_TBT_ML	DP_80D	DP_TX	DP_TBTSNK1_ML_N<3..0>	25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_P<3..0>	5 18 25
	DP_80D	DP_TX	DP_TBTSNK1_ML_C_N<3..0>	5 18 25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_P	25
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_N	25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_P	13 18 25
	DP_80D	DP_AUX	DP_TBTSNK1_AUXCH_C_N	13 18 25
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>	58 62
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>	58 62
	DP_80D	DP_TX	DP_INT_ML_C_P<3..0>	5 58 62
	DP_80D	DP_TX	DP_INT_ML_C_N<3..0>	5 58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P	58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N	58 62
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_P	5 58
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUXCH_C_N	5 58
	DP_80D	DP_AUX	DP_INT_AUXCH_P	
	DP_80D	DP_AUX	DP_INT_AUXCH_N	

PCIe SSD

DP

SYNC_MASTER=J43_MLB SYNC_DATE=09/21/2012

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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA 80D	*	80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA ICOMP	*	=4x DIELECTRIC	?

SOURCE 471984 Chief River MS PDG 1 0 and the spacing rule is adjusted per SI team feedback

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH USB RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB 80D	*	80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP BOTTOM	=4x DIELECTRIC	?

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USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3 PCH TX	USB3 PCH TX	*	USB3 TX2TX
USB3 PCH RX	USB3 PCH RX	*	USB3 RX2RX
USB3 PCH TX	* PCH TX	*	USB3 TX2OTHERTX
USB3 PCH RX	* PCH RX	*	USB3 RX2OTHERRX
USB3 PCH TX	* PCH RX	*	USB3 TX2RX
USB3 PCH RX	* PCH TX	*	USB3 RX2TX
USB3 PCH TX	* TX	*	USB3 2OTHERHS
USB3 PCH RX	* TX	*	USB3 2OTHERHS
USB3 PCH TX	* RX	*	USB3 2OTHERHS
USB3 PCH RX	* RX	*	USB3 2OTHERHS
USB3 PCH TX	*	*	USB3 2OTHER
USB3 PCH RX	*	*	USB3 2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3 TX2TX	TOP BOTTOM	=5x DIELECTRIC	?
USB3 RX2RX	TOP BOTTOM	=5x DIELECTRIC	?
USB3 TX2OTHERTX	TOP BOTTOM	=5x DIELECTRIC	?
USB3 RX2OTHERRX	TOP BOTTOM	=5x DIELECTRIC	?
USB3 TX2RX	TOP BOTTOM	=7x DIELECTRIC	?
USB3 RX2TX	TOP BOTTOM	=7x DIELECTRIC	?
USB3 2OTHERHS	TOP BOTTOM	=6x DIELECTRIC	?
USB3 2OTHER	TOP BOTTOM	=5x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3 TX2TX	*	=2 5x DIELECTRIC	?
USB3 RX2RX	*	=2 5x DIELECTRIC	?
USB3 TX2OTHERTX	*	=4x DIELECTRIC	?
USB3 RX2OTHERRX	*	=4x DIELECTRIC	?
USB3 TX2RX	*	=6x DIELECTRIC	?
USB3 RX2TX	*	=6x DIELECTRIC	?
USB3 2OTHERHS	*	=4x DIELECTRIC	?
USB3 2OTHER	*	=3x DIELECTRIC	?

SOURCE 471984 Cheif River MS PDG 1 0 and the spacing rule is adjusted per SI team feedback

PCH Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_P	
USB_HUB1_UP	USB_80D	USB	USB_HUB_UP_N	
USB_BT	USB_80D	USB	USB_BT_P	14 29
USB_BT	USB_80D	USB	USB_BT_N	14 29
	USB_80D	USB	USB_BT_CONN_P	29 62
	USB_80D	USB	USB_BT_CONN_N	29 62
	USB_80D	USB	USB_BT_WAKE_P	
	USB_80D	USB	USB_BT_WAKE_N	
USB_TPAD	USB_80D	USB	USB_TPAD_P	14 34 62
USB_TPAD	USB_80D	USB	USB_TPAD_N	14 34 62
	USB_80D	USB	USB_TPAD_CONN_P	
	USB_80D	USB	USB_TPAD_CONN_N	
	USB_80D	USB	TPAD_SPI_MOSI_USB_P	
	USB_80D	USB	TPAD_SPI_MISO_USB_N	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_P	
USB_TPAD_M	USB_80D	USB	USB_TPAD_M_N	
USB_SDCARD	USB_80D	USB	USB_SDCARD_P	
USB_SDCARD	USB_80D	USB	USB_SDCARD_N	
	SPI_45S	SPI	TPAD_SPI_MOSI	15 34
	SPI_45S	SPI	TPAD_SPI_MISO	15 34
	SPI_45S	SPI	TPAD_SPI_CLK	15 34
USB_EXTA	USB_80D	USB	USB_EXTA_P	14 33
USB_EXTA	USB_80D	USB	USB_EXTA_N	14 33
	UART_45S	UART	SMC_DEBUGPRT_TX_L	33 35 36
	UART_45S	UART	SMC_DEBUGPRT_RX_L	33 35 36
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_P	33
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_N	33
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_P	33
USB2_EXTA	USB_80D	USB	USB2_EXTA_MUXED_F_N	33
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_P	14 33
USB3_EXTA_RX	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_N	14 33
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_P	33
USB3_EXTA_TX	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_N	33
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_P	
	USB_80D	USB3_PCH_RX	USB3_EXTA_D2R_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_P	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_F_N	
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_P	14 33
	USB_80D	USB3_PCH_TX	USB3_EXTA_R2D_C_N	14 33
USB_EXTB	USB_80D	USB	USB_EXTB_P	14 59 63
USB_EXTB	USB_80D	USB	USB_EXTB_N	14 59 63
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_P	14 59 63
USB3_EXTB_RX	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_N	14 59 63
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_P	59 63
	USB_80D	USB3_PCH_RX	USB3_EXTB_D2R_RC_N	59 63
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_P	59 63
USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_N	59 63
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_P	14 59 63
	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_C_N	14 59 63
USB3_SD_RX	USB_80D	USB3_PCH_RX	NC_USB3RPCIE_SD_D2RP	14 63
USB3_SD_RX	USB_80D	USB3_PCH_RX	NC_USB3RPCIE_SD_D2RN	14 63
USB3_SD_TX	USB_80D	USB3_PCH_TX	NC_USB3RPCIE_SD_R2D_CP	14 63
USB3_SD_TX	USB_80D	USB3_PCH_TX	NC_USB3RPCIE_SD_R2D_CN	14 63
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P	
	USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N	
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_P	
	USB_80D	USB3_PCH_TX	USB3_SD_R2D_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	14
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_PCH_N	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK96M_DOT_N	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_P	
PCH_DIFFCLK_UNUSED	CLK_PCIE_80D	CLK_PCIE	PCH_CLK100M_SATA_N	
	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	

USB Hucopyb nets

TP SPI nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

SYNC_MASTER=CLEAN_J41 SYNC_DATE=11/13/2012

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD
CLK LPC 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	=3x DIELECTRIC	?
CLK LPC	*	=4x DIELECTRIC	?

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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB 45S R 50S	TOP BOTTOM	=50 OHM SE	=50 OHM SE	=50 OHM SE	=50 OHM SE		
SMB 45S R 50S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x DIELECTRIC	?

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SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK SLOW 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK SLOW	*	=4x DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	=4x DIELECTRIC	?

XDP Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH ITP	*	=2 1 SPACING	?

DisplayPort

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP 80D	*	80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP 2DP	*	=3x DIELECTRIC	?
DP 2OTHERHS	*	=4x DIELECTRIC	?
DP 2OTHER	*	=3x DIELECTRIC	?
DP AUX	*	=3x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP 2DP	TOP BOTTOM	=4x DIELECTRIC	?
DP 2OTHERHS	TOP BOTTOM	=6x DIELECTRIC	?
DP 2OTHER	TOP BOTTOM	=4x DIELECTRIC	?
DP AUX	TOP BOTTOM	=4x DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP TX	DP TX	*	DP 2DP
DP TX	* TX	*	DP 2OTHERHS
DP TX	* RX	*	DP 2OTHERHS
DP TX	*	*	DP 2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK SLOW 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD
CLK 25M 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK SLOW	*	=2x DIELECTRIC	?
CLK 25M	*	=5x DIELECTRIC	?

NOTE 25MHz system clocks very sensitive to noise

PCH Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14 35 62
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	14 35 62
	LPC_45S	LPC	LPCPLUS_RESET_L	62
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17 35
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12 17
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS	
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS_R	
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	14 16 19 38 54
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	14 16 19 38 54
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	14 38
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	14 38
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 32 35 38 41 42 62 71
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 32 35 38 41 42 62 71
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12 59 63
	HDA_45S	HDA	HDA_BIT_CLK_R	12
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12 59 63
	HDA_45S	HDA	HDA_SYNC_R	12
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	12
	HDA_45S	HDA	HDA_RST_L	12 59 63
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	12 59 63
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12 59 63
	HDA_45S	HDA	HDA_SDOUT_R	12 17
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	13 36
	CLK_SLOW_45S	CLK_SLOW	SMC_CLK32K	35 36
SPI_CLK	SPI_45S	SPI	SPI_CLK_R	14 44
	SPI_45S	SPI	SPI_CLK	44
SPI_MOSI	SPI_45S	SPI	SPI_MOSI_R	14 44
	SPI_45S	SPI	SPI_MOSI	44
SPI_MISO	SPI_45S	SPI	SPI_MISO	14 44
	SPI_45S	SPI	SPI_MISO_R	44
SPI_CS0	SPI_45S	SPI	SPI_CS0_R_L	14 44
	SPI_45S	SPI	SPI_CS0_L	44
	SPI_45S	SPI	SPI_SMC_CLK	35 44
	SPI_45S	SPI	SPI_SMC_MOSI	35 44
	SPI_45S	SPI	SPI_SMC_MISO	35 44
	SPI_45S	SPI	SPI_SMC_CS_L	35 44
	SPI_45S	SPI	SPI_MLB_CLK	44
	SPI_45S	SPI	SPI_MLB_IO2_WP_L	44
	SPI_45S	SPI	SPI_MLB_IO3_HOLD_L	44
	SPI_45S	SPI	SPI_MLB_CS_L	44
	SPI_45S	SPI	SPI_IO<2>	14 44
	SPI_45S	SPI	SPI_IO2_R	44
	SPI_45S	SPI	SPI_IO<3>	14 44
	SPI_45S	SPI	SPI_IO3_R	44
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	29 62
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	29 62
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	14 29
	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	14 29
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	14 29 62
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	14 29 62
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	12 29 62
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	12 29 62
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>	25
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>	25
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	14 25
	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	14 25
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>	14 25
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	25
	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>	25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	12 25
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	12 25
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_P	
	CLK_PCIE_80D	CLK_PCIE	PEG_CLK100M_N	
XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI	12 16 62
XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO	12 16 62
XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS	12 16 62
XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK	12 16 62
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P	31 32
PCIE_CAM	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N	31 32
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P	14 32
	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P	14 32
PCIE_CAM	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N	14 32
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P	31 32
	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N	31 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	12 32
PCIE_CLK100M_CAM	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	12 32
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	31 32
	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	31 32

Clock Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1	
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	17 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP	31 32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	32
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	31 32
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	17 25
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	25
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	17
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	17
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	17
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2	
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R	
	CLK_25M_45S	CLK_25M	SDSCLK_CLK25M_X1	

SYNC_MASTER=J43_MLB SYNC_DATE=09/14/2012

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40 OHM SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50 OHM SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70 OHM DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_73D	*	=73 OHM DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM DATA2SELF	*	=2x_DIELECTRIC	?
MEM DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM DQS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM CMD2CTRL	*	=3x_DIELECTRIC	?
MEM CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM 2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_73D
MEM_40S	MEM_TERM	MEM_50S

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM 2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER
MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM 2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM 2OTHERMEM

Memory Net Properties

ELECTRICAL CONSTRAINT SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>	7 20 24
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>	7 20 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>	7 21 24
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>	7 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_CS_L<1..0>	7 20 21 24
MEM_A_CTRL	MEM_40S	MEM_CTRL	MEM_A_ODT<0>	7 20 21 24 61
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>	7 20 24
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>	7 21 24
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>	7 20 24 61
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>	7 21 24 61
MEM_A_DQ_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DQ<7..0>	7 61
MEM_A_DQ_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DQ<15..8>	7 61
MEM_A_DQ_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DQ<23..16>	7 61
MEM_A_DQ_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DQ<31..24>	7 61
MEM_A_DQ_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DQ<39..32>	7 21 61
MEM_A_DQ_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DQ<47..40>	7 61
MEM_A_DQ_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DQ<55..48>	7 61
MEM_A_DQ_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DQ<63..56>	7 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 61
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>	7 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 61
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>	7 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 61
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>	7 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 61
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>	7 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 61
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>	7 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 61
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>	7 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 21 61
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>	7 21 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 61
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>	7 61
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>	7 22 24
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>	7 22 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>	7 23 24
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>	7 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_CS_L<1..0>	7 22 23 24
MEM_B_CTRL	MEM_40S	MEM_CTRL	MEM_B_ODT<0>	7 22 23 24 61
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>	7 22 24
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>	7 23 24
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>	7 22 24 61
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>	7 23 24 61
MEM_B_DQ_BYTE0	MEM_40S	MEM_B_DATA_0	MEM_B_DQ<7..0>	7 61
MEM_B_DQ_BYTE1	MEM_40S	MEM_B_DATA_1	MEM_B_DQ<15..8>	7 61
MEM_B_DQ_BYTE2	MEM_40S	MEM_B_DATA_2	MEM_B_DQ<23..16>	7 61
MEM_B_DQ_BYTE3	MEM_40S	MEM_B_DATA_3	MEM_B_DQ<31..24>	7 61
MEM_B_DQ_BYTE4	MEM_40S	MEM_B_DATA_4	MEM_B_DQ<39..32>	7 23 61
MEM_B_DQ_BYTE5	MEM_40S	MEM_B_DATA_5	MEM_B_DQ<47..40>	7 61
MEM_B_DQ_BYTE6	MEM_40S	MEM_B_DATA_6	MEM_B_DQ<55..48>	7 61
MEM_B_DQ_BYTE7	MEM_40S	MEM_B_DATA_7	MEM_B_DQ<63..56>	7 61
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 61
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>	7 61
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 61
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>	7 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 61
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>	7 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 61
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>	7 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 61
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>	7 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 61
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>	7 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 23 61
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>	7 23 61
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 61
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_N<7>	7 61
	MEM_PWR		PP1V2_S3	17 19 20 21 22 23 40 61 69
	MEM_PWR		PP0V6_S3_MEM_VREFCA_A	18 19 20 21
	MEM_PWR		PP0V6_S3_MEM_VREFDQ_A	18 19 20 21
	MEM_PWR		PP0V6_S3_MEM_VREFCA_B	18 19 22 23
	MEM_PWR		PP0V6_S3_MEM_VREFDQ_B	18 19 22 23

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT SPI 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT SPI	*	=2x DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP 80D	*	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF	=80 OHM DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP TX	TBTDP TX	*	TBTDP TX2TX
TBTDP RX	TBTDP RX	*	TBTDP RX2RX
TBTDP TX	TBTDP RX	*	TBTDP TX2RX
TBTDP RX	TBTDP TX	*	TBTDP TX2RX
TBTDP TX	* TX	*	TBTDP 2OTHERHS
TBTDP RX	* TX	*	TBTDP 2OTHERHS
TBTDP TX	* RX	*	TBTDP 2OTHERHS
TBTDP RX	* RX	*	TBTDP 2OTHERHS
TBTDP TX	*	*	TBTDP 2OTHER
TBTDP RX	*	*	TBTDP 2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP TX2TX	TOP BOTTOM	=6x DIELECTRIC	?
TBTDP RX2RX	TOP BOTTOM	=6x DIELECTRIC	?
TBTDP TX2RX	TOP BOTTOM	=10x DIELECTRIC	?
TBTDP 2OTHERHS	TOP BOTTOM	=10x DIELECTRIC	?
TBTDP 2OTHER	TOP BOTTOM	=6x DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP TX2TX	*	=4x DIELECTRIC	?
TBTDP RX2RX	*	=4x DIELECTRIC	?
TBTDP TX2RX	*	=6x DIELECTRIC	?
TBTDP 2OTHERHS	*	=6x DIELECTRIC	?
TBTDP 2OTHER	*	=4x DIELECTRIC	?

Thunderbolt/DP Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_P<1..0>	25 28
TBT_A_R2D	TBTDP_80D	TBTDP_TX	TBT_A_R2D_C_N<1..0>	25 28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_P<1..0>	28
	TBTDP_80D	TBTDP_TX	TBT_A_R2D_N<1..0>	28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_P<1>	25 28
DP_TBTPA_ML1	DP_80D	DP_TX	DP_TBTPA_ML_C_N<1>	25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_P<3>	25 28
DP_TBTPA_ML3	DP_80D	DP_TX	DP_TBTPA_ML_C_N<3>	25 28
	DP_80D	DP_TX	DP_TBTPA_ML_P<3..1:2>	28
	DP_80D	DP_TX	DP_TBTPA_ML_N<3..1:2>	28
	DP_80D	DP_TX	DP_A_LSX_ML_P<1>	28
	DP_80D	DP_TX	DP_A_LSX_ML_N<1>	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_P<1..0>	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R_C_N<1..0>	28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<1>	25 28
TBT_A_D2R1	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<1>	25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_P<0>	25 28
TBT_A_D2R0	TBTDP_80D	TBTDP_RX	TBT_A_D2R_N<0>	25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_P	25 28
TBT_A_AUXCH	DP_80D	DP_AUX	DP_TBTPA_AUXCH_C_N	25 28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_P	28
	DP_80D	DP_AUX	DP_TBTPA_AUXCH_N	28
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_A_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_P	28
	TBTDP_80D	TBTDP_RX	TBT_A_D2R1_AUXDDC_N	28
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_P<1..0>	62
TBT_B_R2D	TBTDP_80D	TBTDP_TX	TBT_B_R2D_C_N<1..0>	62
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_P<1..0>	
	TBTDP_80D	TBTDP_TX	TBT_B_R2D_N<1..0>	
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CP<3..1:2>	62
DP_TBTPB_ML	DP_80D	DP_TX	NC_DP_TBTPB_ML_CN<3..1:2>	62
	DP_80D	DP_TX	DP_TBTPB_ML_P<3..1:2>	
	DP_80D	DP_TX	DP_TBTPB_ML_N<3..1:2>	
	DP_80D	DP_TX	DP_B_LSX_ML_P<1>	
	DP_80D	DP_TX	DP_B_LSX_ML_N<1>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_P<1..0>	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R_C_N<1..0>	
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_P<1..0>	62
TBT_B_D2R	TBTDP_80D	TBTDP_RX	TBT_B_D2R_N<1..0>	62
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CP	25 62
TBT_B_AUXCH	DP_80D	DP_AUX	NC_DP_TBTPB_AUXCH_CN	25 62
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_P	
	DP_80D	DP_AUX	DP_TBTPB_AUXCH_N	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_P	
	DP_80D	DP_AUX	DP_B_AUXCH_DDC_N	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_P	
	TBTDP_80D	TBTDP_RX	TBT_B_D2R1_AUXDDC_N	

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
	DP_80D	DP_TX	DP_TBTSRC_ML_C_P<3..0>	
	DP_80D	DP_TX	DP_TBTSRC_ML_C_N<3..0>	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_P	
	DP_80D	DP_AUX	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	25
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	25
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	25
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	25

Only used on hosts supporting Thunderbolt video-in

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI 85D	*	85_OHM_DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF	85 OHM DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI 2OTHER	*	4X DIELECTRIC	?
MIPI 2CLK	*	6X DIELECTRIC	?
MIPICLK 2OTHER	*	7X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI 2OTHER	TOP BOTTOM	6X DIELECTRIC	?
MIPI 2CLK	TOP BOTTOM	8X DIELECTRIC	?
MIPICLK 2OTHER	TOP BOTTOM	10X DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI DATA	*	*	MIPI 2OTHER
MIPI DATA	CLK MIPI	*	MIPI 2CLK
CLK MIPI	*	*	MIPICLK 2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2 MEM 45S	*	=45 OHM SE	=45 OHM SE	=45 OHM SE	=45 OHM SE	=STANDARD	=STANDARD
S2 MEM 85D	*	85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF	=85 OHM DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2 DATA2SELF	*	=2x_DIELECTRIC	?
S2 DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2 CMD2CTRL	*	=2x_DIELECTRIC	?
S2 CTRL2CTRL	*	=2x_DIELECTRIC	?
S2 2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM 2PWR	*	=2x_DIELECTRIC	?
S2MEM 2GND	*	=2x_DIELECTRIC	?
S2MEM 2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2 DATA2SELF	TOP BOTTOM	=4x DIELECTRIC	?
S2 DQS2OWNDATA	TOP BOTTOM	=4x DIELECTRIC	?
S2_CMD2CMD	TOP BOTTOM	=4x DIELECTRIC	?
S2 CMD2CTRL	TOP BOTTOM	=4x DIELECTRIC	?
S2 CTRL2CTRL	TOP BOTTOM	=4x DIELECTRIC	?
S2 2OTHERMEM	TOP BOTTOM	=6x DIELECTRIC	?
S2MEM 2PWR	TOP BOTTOM	=4x DIELECTRIC	?
S2MEM 2GND	TOP BOTTOM	=4x DIELECTRIC	?
S2MEM 2OTHER	TOP BOTTOM	=10x DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2 MEM DATA*	*	*	S2MEM 2OTHER
S2 MEM DQS*	*	*	S2MEM 2OTHER
S2_MEM_CMD	*	*	S2MEM 2OTHER
S2_MEM_CTRL	*	*	S2MEM 2OTHER
S2_MEM_CLK	*	*	S2MEM 2OTHER
S2 MEM DATA*	=SAME	*	S2 DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2 CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2 CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2 2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2 MEM DATA1	*	S2 DQS2OWNDATA
S2_MEM_DQS0	S2 MEM DATA0	*	S2 DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	31 32
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	31 32
S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	31 32
	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	31 32
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	32 62
	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	32 62
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	31 32
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	31 32
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	32 62
	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	32 62
		S2_MEM_PWR	PP1V35_CAM	31 32
		S2_MEM_PWR	PP0V675_CAM_VREF	31 32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA	32
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ	32

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1 DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0 1 MM	0 1 MM
2TO1 DIFFPAIR	*	=STANDARD	0 2 MM	0 1 MM	=STANDARD	0 1 MM	0 1 MM

SMC SMBus Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
SMBUS_SMC_0_S0_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_0_S0_SCL	35 38 58
SMBUS_SMC_0_S0_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_0_S0_SDA	35 38 58
SMBUS_SMC_1_S0_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14 32 35 38 41 42 62 67
SMBUS_SMC_1_S0_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14 32 35 38 41 42 62 67
SMBUS_SMC_2_S3_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_2_S3_SCL	35 38 59 63
SMBUS_SMC_2_S3_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_2_S3_SDA	35 38 59 63
SMBUS_SMC_3_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_3_SCL	34 35 38 42 62
SMBUS_SMC_3_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_3_SDA	34 35 38 42 62
SMBUS_SMC_5_G3_SCL	SMB_455_R_50S	SMB	SMBUS_SMC_5_G3_SCL	35 38 46 48 62
SMBUS_SMC_5_G3_SDA	SMB_455_R_50S	SMB	SMBUS_SMC_5_G3_SDA	35 38 46 48 62

SMBus Charger Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE PHYSICAL	NET TYPE SPACING		
SENSE_DIFFPAIR			CHGR_CSI_P	48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSI_N	48
	2TO1_DIFFPAIR		CHGR_CSI_R_P	48
	2TO1_DIFFPAIR		CHGR_CSI_R_N	48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_P	48
SENSE_DIFFPAIR	2TO1_DIFFPAIR		CHGR_CSO_N	48
	2TO1_DIFFPAIR		CHGR_CSO_R_P	41 48
	2TO1_DIFFPAIR		CHGR_CSO_R_N	41 48

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE 1TO1 45S	*	1TO1 DIFFPAIR	=45 OHM SE	=45 OHM SE	=45 OHM SE	=1TO1 DIFFPAIR	=1TO1 DIFFPAIR
SENSE 1TO1 P2MM	*	1TO1 DIFFPAIR	0 200 MM	0 100 MM	=1TO1 DIFFPAIR	=1TO1 DIFFPAIR	=1TO1 DIFFPAIR
THERM 1TO1 45S	*	1TO1 DIFFPAIR	=45 OHM SE	=45 OHM SE	=45 OHM SE	=1TO1 DIFFPAIR	=1TO1 DIFFPAIR
SPKR DIFFPAIR	*	1TO1 DIFFPAIR	0 300 MM	0 100 MM	=1TO1 DIFFPAIR	=1TO1 DIFFPAIR	=1TO1 DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2 1 SPACING	?
THERM	*	=2 1 SPACING	?
AUDIO	*	=2 1 SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND P2MM	*	0 20 MM	10000
PWR P2MM	*	0 20 MM	10000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU COMP	GND	*	GND P2MM
CPU VCCSENSE	GND	*	GND P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK PCIE	*	GND P2MM
GND	PCIE*	*	GND P2MM
GND	SATA*	*	GND P2MM
GND	USB*	*	GND P2MM
GND	LVDS*	*	GND P2MM
SB POWER	CLK PCIE	*	PWR P2MM
SB POWER	SATA*	*	PWR P2MM
SB POWER	SATA*	*	PWR P2MM

J11/J13 Specific Net Properties

ELECTRICAL CONSTRAINT SET	NET TYPE: PHYSICAL	NET TYPE: SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	INLET_THMSNS_D1_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_R_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBTTHMSNS_D2_N	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_P	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_MLBBOT_THMSNS_N	42
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	MLBBOT_THMSNS_D3_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_P	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	TBDTHMSNS_D2_N	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_P	42
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUTHMSNS_D2_N	42
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_N	
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVCCIOS0_CS_P	
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P	40 50
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N	40 50
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_P	40 50
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	CPUVR_ISNS2_N	40 50
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_P_R	40 41
	SENSE_1TO1_P2MM	SENSE	CPUVR_ISNS1_N_R	40 41
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_P	40
	SENSE_1TO1_45S	SENSE	CPUVR_ISUM_R_N	40
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_P	40
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_CPUDDR_N	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_N	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3S5_P	40
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_3V3_S0_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_CAMERA_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_P3V3_S0_P	39
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_P	40 53
SENSE_DIFFPAIR	SENSE_1TO1_P2MM	SENSE	ISNS_1V05_S0_N	40 53
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_BMON_GAIN_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	39 41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	39 41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_N	39 51
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V2_S3_P	39 51
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	39
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_N	41
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PANEL_P	41
DIFF	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_N	41 42
DIFF	SENSE_1TO1_45S	SENSE	ISNS_HS_GAIN_P	41 42
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	45 59 63
AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	45 59 63
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_P	45
	1TO1_DIFFPAIR	AUDIO	MAX98300_R_N	45
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	45 62
SPKR_OUT	SPKR_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	45 62
		SB_POWER	PP3V3_S5	8 11 13 15 16 17 18 28 29 49 52 60 62 63
		SB_POWER	PP3V3_S0	8 11 13 13 15 17 18 26 30 34 36 37 38 39 40 41 42 43 54 57 59
	GND		GND	

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